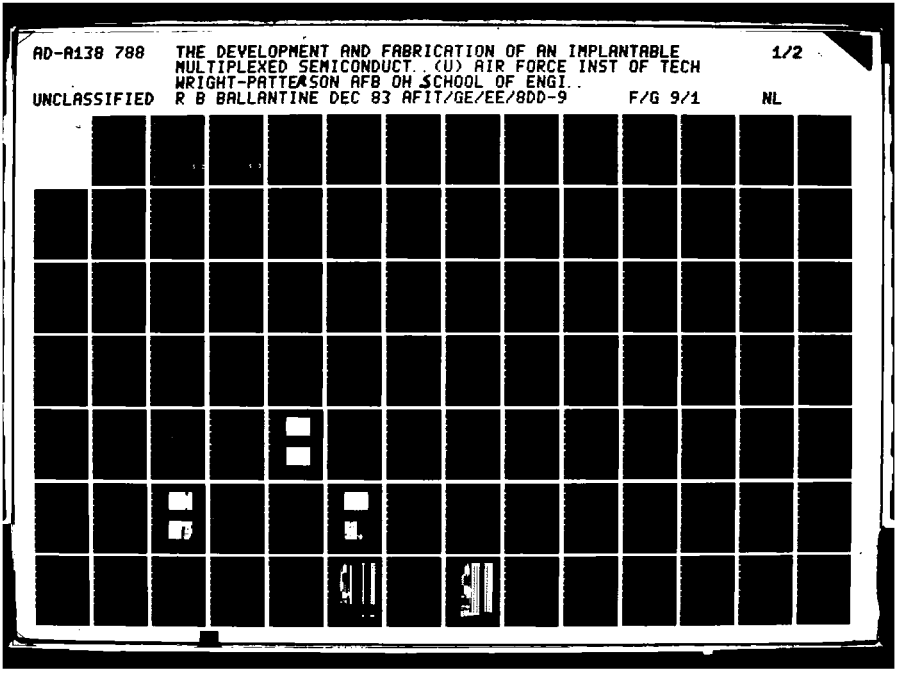
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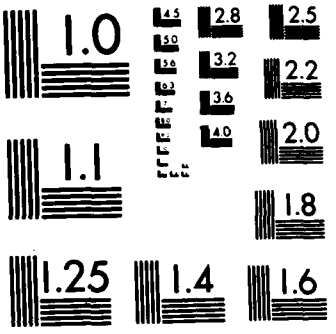

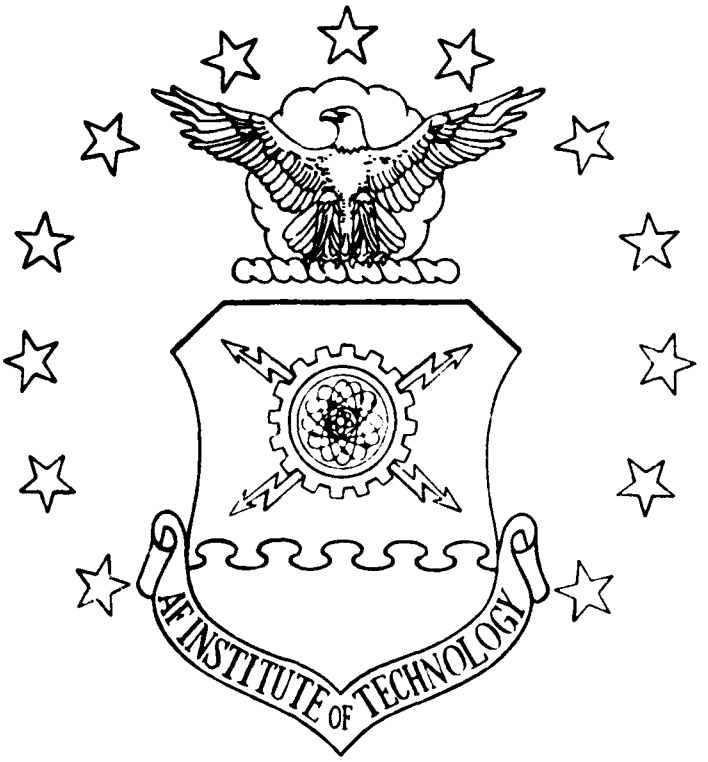

THE DEVELOPMENT AND FABRICATION OF AN IMPLANTABLE, MULTIPLEXED, SEMICONDUCTOR MULTIELECTRODE ARRAY

THESIS

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THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

by

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Preface

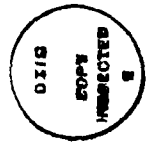
The intent of this thesis project is to fabricate an implantable, multiplexed, multielectrode array based on work previously accomplished by 2Lt J. A. Tatman, Capt G. H. Fitzgerald, Capt G. W. German, Capt R. W. Hensley and 1Lt D. C. Denton. Their individual and collective efforts in designing, fabricating, and testing an implantable array resulted in a semiconductor device suitable for implanting, monitoring, and recording cortical signals produced by visual stimulation. The analysis and understanding of these recorded signals are crucial if science is to understand the principles of pattern recognition by which the brain processes information.

This thesis involves two main areas: First, fabrication of a multielectrode array, and second, design and incorporation of a multiplexer with the multielectrode array. The array fabrication uses the original Tatman mask design, but is fabricated using an entirely different series of processes. The multiplexer design is a parallel effort, and is intended to replace a previously designed, but non-functioning multiplexer.

I wish to thank Capt Roger Colvin, thesis advisor, and Mr. Donald Smith, electronics technician, for their continuing suggestions, guidance, support, and encouragement during the course of this effort. I would also like to thank Mr. Thomas Herbert, 1Lt Robert Bellacicco, A1C Greg Creech and Mr. Mike Powell of the Avionics Laboratory for

their assistance. In addition, I wish to extend my appreciation to Dr. Matthew Kabrisky and Capt Russell Hensley for their valuable advice, as thesis committee members, in the preparation of this thesis.

Robert B. Ballantine



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Abstract

A new JFET multielectrode array, consisting of a four by four array and sixteen junction field effect transistors, has been fabricated. Changes in the fabrication processes include: The use of three inch wafers, in lieu of one and one quarter inch wafers; positive photoresist, instead of negative photoresist; different impurity sources; diffe nt diffusion times and temperatures; and a two m al metallization layer, versus a four metal metalliza i layer.

In addition, two unique NMOS multiplexer circuits have been designed for use with either the JFET multielectrode array, or an NMOS multielectrode array. The first multiplexer circuit contains a count-selectable counter, a one of sixteen output multiplexer, a decoder for generating a sync signal, and a sixteen by sixteen multielectrode array, all on a single chip. In addition, the array can be separated from the chip, permitting the use of the remaining circuitry with other types and sizes of arrays.

The second multiplexer circuit contains the same features of the first multiplexer, plus an additional one of sixteen output multiplexer and a four-bit counter. With this chip, however, the array can not be separated from the remaining circuitry.

THE DEVELOPMENT AND FABRICATION OF AN IMPLANTABLE, MULTIPLEXED, SEMICONDUCTOR MULTIELECTRODE ARRAY

CHAPTER I

INTRODUCTION

Background

Considerable research effort is being expended in an effort to understand the human brain's visual pattern recognition processes. That is, the processes by which the human brain determines that an 8, 8, or 8 is meant to be the number eight. So far no machine has been built with such a differentiating capability. However, with further detailed study, and understanding of these pattern recognition processes, a machine could be built with even the complex capability of identifying a specific object in a complex visual scene. In addition, this understanding could lead to developing a visual prosthesis, enabling many of the world's blind people to see. Obtaining an adequate understanding of these processes requires simultaneous reco.ding of hundreds to thousands of signals from the visual cortex of a living, seeing, biological specimen, over a relatively long period of time (weeks to months).

Currently, the two most common methods of recording cortical signals are electroencephalograms (EEG), and direct cortical exploration. With the EEG method, recording

electrodes are attached to the skull, in a specific pattern, and detect electrical pulses radiated by the cortex. The signals are transmitted by wire leads to a remote recording device. Analyzing visual information processes of the brain by the EEG method can be compared to analyzing the functions of a computer by monitoring the varying electromagnetic fields surrounding the computer's chassis; a lot of data gathered, though not very meaningful or useful.

On the other hand, recording signals from the visual cortex by direct cortical examination requires very small electrical probes be placed on the surface of the visual cortex. While this method enables one to record visual signals right at the source, using such probe devices introduces several undesirable constraints. First, positioning the probes on the surface of the visual cortex requires an opening be made and left open through the skull so the probes' electrical leads can be connected to an external recording device. This opening inevitably leads to infection, regardless of the precautions taken. Second, increasing the number of probes increases the required number of electrical leads. An increase in the number of leads requires a larger opening, increasing the risk of infection, and increasing the problem of managing numerous fine wires. Third, using a probe device increases the possibility of physically damaging the delicate cortical tissue. Fourth, recording useful information directly from the cortex requires that the probes be no larger than the

basic computing elements (BCE) of the cortex. The BCEs are considered to be the fundamental areas for processing visual stimuli, and are believed to be on the order of 0.05 millimeters to 0.5 millimeters in diameter (Ref 1:133). Manufacturing electrodes the size of the BCE is extremely difficult.

These constraints make small electrical probes highly unsuitable as long term recording electrodes. What is required is a small device capable of being surgically implanted under the skull and in contact with the cortex. A small device so located could sense numerous BCE visual signals, and pass the information across an intact scalp to an external recording device.

Just such a device was proposed by Dr. Borky, of the Air Force Institute of Technology, and designed by Tatman (Ref 2). It was Tatman's conceptual idea to design and fabricate a silicon chip integrated circuit consisting of: an electrode array (n-rows by m-columns) expandable to several thousand electrodes; dedicated junction field effect transistors (JFET) functioning as on-off switches for each electrode; matrix multiplexing the array to a single output; and outputting the data across an intact scalp by using a low power tunnel diode RF transmitter (Ref 2:16). Additional circuitry, such as a driving circuit providing circuit control and timing, could be incorporated on the chip with all required power being supplied by an implantable power supply such as is used in a heart

pacemaker.

Tatman actually designed and fabricated a four by four electrode array with sixteen JFETs, and nine signal wires. One wire provided a common ground between the brain and external electronics, four wires were used to externally multiplex the rows of the array, and four wires connected the array column outputs to an external recording device. Tatman chose this design because it greatly simplified fabricating the initial device, making the feasibility study less complicated.

This initial design was conceptually simple. The gates of each of the four JFETs in a row were tied together and connected to one of the external multiplexer channels; the source of each JFET was tied to one of the array electrodes; and the drains of each of the four JFETs in a column were tied together and connected to one of the external recording channels. When the gate of any JFET is turned on, any signal present at the electrode (source), will also appear at the output (drain). Tatman had several problems fabricating the device, resulting from inadequate temperatures and times in his processing schedule, and did not produce a functioning integrated circuit chip.

In 1980, Fitzgerald modified Tatman's processing schedule and produced a device that functioned properly in air, but did not function in saline (a salt solution similiar to the cerebrospinal fluid surrounding the brain). Fitzgerald believed the problem to be pinholes in the

passivation layer, through which contaminating sodium ions were attracted by the electrical field developed by the JFET pinch-off voltage. These sodium ions produced leakage paths between the metal leads, shorting out the circuitry (Ref 3:109). The passivation problem was worked out by German (Ref 4), and a functioning "brain chip" was implanted in a biological specimen (dog) by Hensley and Denton (Ref 5).

Summary of Current Knowledge

Hensley and Denton showed the feasibility of Tatman's basic multielectrode design by implanting the device in a living, seeing, biological specimen, and recording visually evoked signals from the visual cortex over a 19 day period.

The overall efforts of Tatman, Fitzgerald, German, Hensley, and Denton also showed that current integrated circuit fabrication techniques are suitable for fabricating a device such as the brain chip. These techniques, using silicon wafers to produce integrated circuit chips, are well developed and understood, and lend themselves to fabricating devices with dimensions required of the brain chip. These techniques will make fabricating the complex version of Tatman's brain chip feasible, providing each of the individual circuit elements (drive circuit, transmitter, etc.) are compatible with all the other circuit elements. Thus, designing and fabricating the additional circuit elements within the size limitations of the brain chip are

possible.

Statement of the Problem

The purpose of this thesis was to fabricate the next generation brain chip, with a multiplexer circuit, as the next step toward a totally implantable device. The primary problem was to fabricate a new batch of four by four electrode arrays, using different processing techniques than those used by Tatman or Fitzgerald. Also, the capability of fabricating a sixteen by sixteen array was needed, thereby requiring a new electrode array layout.

Initially, a multiplexed version of a four by four JFET array had been designed by Bellacicco, LaVoie, and Posten (Ref 6). However, at the time of design layout, suitable graphics plotting was not available, and it was later determined that the multiplexer design would not work because of many "opens" in the metallization layer. These "opens" were due to misalignment of the metal, diffusion, and contact window layers. Therefore, a new multiplexer had to be designed. It was decided that an NMOS, multiplexed, sixteen by sixteen array would be designed with the capability of separating the multiplexer from the array, and using the NMOS multiplexer with the new four by four JFET array. Additionally, the multiplexer could be used with the sixteen by sixteen JFET electrode array, when this array becomes available.

The JFET array fabrication used the same basic mask

design layout as did Tatman's and Fitzgerald's efforts. However, several major changes were incorporated in the processing schedule. These changes introduced new problems associated with size and type of wafers, type of photoresist, type of diffusion sources, use of new diffusion furnaces, use of a new mask aligner, fabrication of a new mask set, and new metallization procedures. Each of these items, with their resulting processes, was different than those previously used, resulting in Fitzgerald's processing schedule (Ref 3:125-131) being greatly modified and therefore of little value in processing, other than as a very general guide. As a result, an entirely new processing schedule had to be created (see Appendix F), taking into consideration all the changes.

Scope

This thesis project involved several major areas, each limited as indicated below. The first area was the design and testing of the NMOS multiplexer, but excluding its fabrication (this was done commercially). The second area was the duplication of the four by four JFET array mask set for use with positive photoresist. A third area was the layout of the new sixteen by sixteen JFET array mask set, and a passivation mask for the NMOS multiplexer. These masks were obtained with the assistance of the Avionics Laboratory, Wright-Patterson AFB. Finally, the fourth area was the fabrication and testing of a four by four JFET

array.

This thesis project did not involve the design of any circuitry to be used in subsequent brain chip designs, nor investigating the suitablity of passivating materials. Neither did it involve the implanting of a device in a biological specimen, nor did it involve the recording of or analyzing of any biological data.

Approach and Presentation

This thesis is primarily oriented toward the fabrication of the four by four JFET array, and is presented in a chronological order.

Chapter II presents the initial calculations required for the fabrication of the JFET array. These calculations include those for the epitaxial layer, isolation, gate, and source/drain diffusions. In addition, calculations of oxide thicknesses required to mask the diffusion processes are included.

Chapter III presents the chronological steps involved in the fabrication. Results of the quality of the thermally grown oxide layer, obtained through capacitance-voltage (C-V) testing methods, are shown. The actual oxide thicknesses, derived from ellipsometer readings, are compared with the calculated thicknesses. Surface resistivity measurements of impurity doping concentrations are shown, and compared to manufacturer's literature. The actual diffusion results, obtained by beveling and staining,

are compared to the calculated results of Chapter II, and midcourse calculation corrections are shown.

Chapter IV presents the results of electrical tests on the array using a transistor curve tracer, and a short analysis of the test results.

Chapter V presents a summary of two different NMOS multiplexer designs. First, Multiplexer Design I is presented, and then Multiplexer Design II is presented. Finally, a summary of the testing of Multiplexer Design I is presented with the final results.

Chapter VI presents the conclusions derived from the fabrication, and some recommendations concerning some of the pitfalls of the fabrication, and what might be done in the future to prevent similiar problems.

Additionally, material that is relevant to the overall thesis project, or specific areas, but not significant enough for inclusion in the main text, is presented in the appendices that follow the main thesis.

CHAPTER II

JFET FABRICATION CALCULATIONS

Introduction

Prior to actually fabricating the brain chip electrode array, various initial calculations must be made to establish a "ball-park" idea of what will occur during the fabrication processes. As stated, these are initial calculations, and will possibly require several revisions as the fabrication processes proceed. The calculations determine:

1. How deep the epitaxial layer will diffuse during the entire process.

2. How deep the isolation diffusion must go to establish isolation.

3. How deep the gate diffusion must go to establish a channel length of one micron or less.

4. How deep the source/drain diffusion must go.

5. How thick the initial oxide must be to mask the isolation, gate, and source/drain diffusions.

6. How thick the gate oxide must be to mask the source/drain diffusion.

These calculations are fairly straight forward. However, most of the processes are interdependant, in that changing one process affects other processes and therefore the calculations for each affected process. The calculations presented in this chapter are the result of

several iterations of all the calculations, using different processing times, in order to meet the JFET design requirements as follows. Every time the wafer is subjected to a high temperature process (oxide growth, diffusion) the epitaxial layer (epi) will diffuse slowly into the substrate because the epi doping is only slightly higher than the substrate. The isolation diffusion must diffuse deeper than the epi in order to achieve isolation. It is desired that the JFET gate diffuse to within one micron or less of the epi, but not diffuse deeper than the epi, to preclude shorting out the gate. It is also desired that the JFET source/drain diffuse roughly one-half the depth of the epi, although there is considerable tolerance in this step. Although the different diffusions are interrelated and at times simultaneous, each diffusion can be calculated separately by considering all processes affecting that diffusion. The first set of calculations shown are those for the epi diffusion.

Calculating Epitaxial Layer Diffusion

The epi diffusion, as well as all other diffusions, is a function of at least four basic parameters: time, temperature, impurity doping concentration gradient, and type of impurity. The longer the time, the deeper the diffusion; and the higher the temperature and the steeper the gradient, the faster the diffusion progresses. Also, given identical conditions, various impurities diffuse at

different rates. The impurity gradient is determined by the difference in impurity doping concentrations at the surface versus the doping concentration in the bulk, or background; the greater the difference, the steeper the gradient.

From the text by Grove, one obtains, after slight manipulation and change of notation, the following equation for epi diffusion (Ref 7:80):

$$N(x,t) = N_{epi}\, 2^{-1}\left[\operatorname{erfc}\langle x_j 2^{-1} (Dt)^{-1/2} \rangle\right] \qquad \text{(II-1)}$$

where

$N(x,t)$ is the impurity concentration as a function of time and diffused length,

N_{epi} is the bulk impurity doping concentration of the epitaxial layer (epi),

x_j is the depth where $N(x,t)$ equals N_b, the bulk, or background concentration,

Dt is the diffusion coefficient, time product, and

erfc is the complimentary error function.

Given that the manufacturer specifies the epi to be 2 microns thick, with a resistivity of .9 ohm-cm, it is determined that the impurity concentration of the epi is 6×10^{15} cm^{-3} (Ref 7:113). The impurity concentration of the substrate, as specified to the manufacturer, is 5×10^{14} cm^{-3}. This is N_b, as the substrate becomes the background into which the epi diffuses.

The erfc is used whenever an infinite source is present in a diffusion. Since the epi is uniformily doped and 2 microns thick, it can be assumed to be an infinite source (Ref 7:67).

Several assumptions/decisions were made in order to obtain the necessary information required to solve equation II-1. First, it was assumed that the n-type epi was doped with phosphorous, and second, it was assumed that the p-type substrate was doped with boron. Next, it was decided to grow the initial oxide and to perform the isolation and gate diffusions at 1050 degrees C. It was also decided that the source/drain diffusion would be performed at 1000 degrees C.

Based on the above assumptions, the diffusion coefficient for phosphorous was determined. Since phosphorous is a donor impurity, the diffusion coefficient for donor impurities was found in Grove (Ref 7:39). Grove, however, specifies only two diffusion coefficients for phosphorous, and both of the coefficients are for high concentrations (10^{19} cm^{-3} and 10^{21} cm^{-3}). Glaser, on the other hand, assumes boron and phosphorous to have the same diffusion coefficients (Ref 8:240). It was decided to make this same assumption and compute Grove's diffusion coefficient for phosphorous at low doping concentrations using his graph for acceptor impurities (boron) (Ref 7:38). This resulted in a diffusion coefficient for phosphorous (after solving for proper units), of 4.9395×10^{-14} $cm^2\text{-}sec^{-1}$ at 1050 degrees C, and 1.4653×10^{-14} $cm^2\text{-}sec^{-1}$ at 1000

degrees C.

Finally, with all the required information, Table II-1 was compiled and equation II-1 solved for the erfc and then x_j, resulting in the following equation:

$$x_j = 1.9560(Dt)^{1/2} \qquad \text{(II-2)}$$

Equation II-2 was then used to compute the epi layer diffused depth at the end of each process. This information is included in Table II-1.

This concluded the initial calculations for the epi diffusion. The next set of calculations determine the isolation diffusion depth.

Calculating Isolation Diffusion

The isolation diffusion consists of a boron predeposition (predep) and an initial drive, plus the drives resulting from subsequent processes. The predep, initial drive, and some of the subsequent drives occur at 1050 degrees C, indicating a diffusion coefficient of 4.9395×10^{-14} $cm^2\text{-}sec^{-1}$. The remaining drives occur at 1000 degrees C, indicating a diffusion coefficient of 1.4653×10^{-14} $cm^2\text{-}sec^{-1}$ (Ref 7:38).

During the isolation predep, a boron source wafer is used to deposit a thin layer of impurities on the surface of the silicon wafers. The impurity doping concentration of this layer is assumed to be the solid solubility limit of

TABLE II-1

Initial Calculations for Epi Diffusion

	D (cm^2-sec^{-1})	t (sec)	Dt (cm^2)	Σ Dt (cm^2)	x_j (μm)
Initial Oxide	4.9395×10^{-14}	5316	2.6258×10^{-10}	2.6258×10^{-10}	.3170
Isolation Predep	"	2400	1.1855×10^{-10}	3.8113×10^{-10}	.3819
Isolation Drive	"	24000	1.1855×10^{-9}	1.5666×10^{-9}	.7742
Gate Predep	"	900	4.4456×10^{-11}	1.6111×10^{-9}	.7851
Gate Drive	"	9600	4.7419×10^{-10}	2.0853×10^{-9}	.8932
Source/Drain Predep	1.4653×10^{-14}	900	1.3188×10^{-11}	2.0985×10^{-9}	.8961
Source/Drain Drive	"	1200	1.7584×10^{-11}	2.1161×10^{-9}	.8998

$$N(x,t) = N_s 2^{-1}(\text{erfc}(x_j 2^{-1}(Dt)^{-1/2}))$$

$$N_s = 6 \times 10^{15}\ cm^{-3}$$

$$N_b = 5 \times 10^{14}\ cm^{-3}$$

the impurity at the temperature at which it is deposited. In this case, boron at 1050 degrees C has a solid solubility limit of $4x10^{20}$ cm^{-3} (Ref 8:241). Additionally, N_b is $6x10^{15}$ cm^{-3} as the boron is diffusing into the epi, and the epi is therefore the background. Using this information, Table II-2 was compiled. Like the epi diffusion, the isolation predep is performed with an infinite source, resulting in an erfc for calculating the diffused depth during the predep. However, unlike the epi diffusion, the impurity doping concentration gradient is very steep, with little or no diffusion of the epi into the isolation. This results in the following equation:

$$N(x,t) = N_o[\text{erfc}\langle x_j 2^{-1}(Dt)^{-1/2}\rangle] \qquad \text{(II-3)}$$

where N_o is the solid solubility limit.

Equation II-3 was solved for the erfc and then x_j, resulting in the following equation:

$$x_j = 6.1218(Dt)^{1/2} \qquad \text{(II-4)}$$

Next, the diffusion depth after each drive was calculated. At this point, the source wafers are no longer present and only the impurities deposited during predep are present to continue diffusing. This thin layer is considered to be a finite source and results in the diffusion following a

TABLE II-2

Initial Calculations for Isolation Diffusion

	D (cm^2-sec^{-1})	t (sec)	Dt (cm^2)	Σ Dt (cm^2)	x_j (μm)
Isolation Predep	4.9395×10^{-14}	2400	1.1855×10^{-10}	1.1855×10^{-10}	.6665
Isolation Drive	"	24000	1.1855×10^{-9}	1.1855×10^{-9}	2.7895
Gate Predep	"	900	4.4456×10^{-11}	1.2300×10^{-9}	2.8268
Gate Drive	"	9600	4.7419×10^{-10}	1.7041×10^{-9}	3.1874
Source/Drain Predep	1.4653×10^{-14}	900	1.3188×10^{-11}	1.7173×10^{-9}	3.1966
Source/Drain Drive	"	1200	1.7584×10^{-11}	1.7349×10^{-9}	3.2089

$$N(x,t) = N_o(\text{erfc}(x_j 2^{-1}(Dt)^{-1/2}))$$

$$Q(t) = 2N_o(Dt)^{1/2}\pi^{-1/2}$$

$$= 4.9143 \times 10^{15}\ cm^{-2}$$

$$N(x,t) = Q(\pi Dt)^{-1/2}(\exp(-x_j^2(4Dt)^{-1}))$$

$$N_o = 4 \times 10^{20}\ cm^{-3}$$

$$N_b = 6 \times 10^{15}\ cm^{-3}$$

gaussian distribution during the drives. The equation for this diffusion is found in Grove (Ref 7:50):

$$N(x,t) = Q(\pi Dt)^{-1/2} \exp[-x_j^2(4Dt)^{-1}] \qquad \text{(II-5)}$$

where Q is the number of atoms deposited during predep.

To find Q, the following equation is used (Ref 7:47).

$$Q(t) = 2N_o(Dt)^{1/2}\pi^{-1/2} \qquad \text{(II-6)}$$

Solving equation II-6 for Q and substituting the value into equation II-5, equation II-5 was solved for the isolation diffusion depths at the end of each process, and equation II-4 was solved for the isolation diffusion depth after the predep. This information is included in Table II-2.

This concluded the initial calculations for the isolation diffusion. The next set of calculations determine the gate diffusion depth.

Calculating Gate Diffusion

Like the isolation diffusion, the gate diffusion consists of a boron predep, initial drive, and subsequent drives at 1050 degrees C and 1000 degrees C into the epi layer. This results in almost the same information for the gate diffusion as for the isolation diffusion. The only difference is Q(t), since the gate predep time is much

TABLE II-3

Initial Calculations for Gate Diffusion

	D (cm^2-sec^{-1})	t (sec)	Dt (cm^2)	Σ Dt (cm^2)	x_j (μm)
Gate Predep	4.9395×10^{-14}	900	4.4456×10^{-11}	4.4456×10^{-11}	.4082
Gate Drive	"	9600	4.7419×10^{-10}	4.7419×10^{-10}	1.7486
Source/Drain Predep	1.4653×10^{-14}	900	1.3188×10^{-11}	4.8738×10^{-10}	1.7661
Source/Drain Drive	"	1200	1.7584×10^{-11}	5.0496×10^{-10}	1.7891

$$N(x,t) = N_o(\text{erfc}(x_j 2^{-1}(Dt)^{-1/2}))$$

$$Q(t) = 2N_o(Dt)^{1/2}\pi^{-1/2}$$

$$= 3.0094 \times 10^{15}\ cm^{-2}$$

$$N(x,t) = Q(\pi Dt)^{-1/2}(\exp(-x_j^2(4Dt)^{-1}))$$

$$N_o = 4 \times 10^{20}\ cm^{-3}$$

$$N_b = 6 \times 10^{15}\ cm^{-3}$$

shorter than the isolation predep time. This information is compiled in Table II-3. Solving equation II-6 for Q, and substituting the value into equation II-5, equation II-5 was solved for the gate diffusion depths after each process, and equation II-4 was solved for the gate diffusion depth after the gate predep. This information is included in Table II-3.

This concluded the initial calculations for the gate diffusion. The next, and final set of calculations determine the source/drain diffusion depth.

Calculating Source/Drain Diffusion

The source/drain diffusion consists only of a phosphorous predep and drive at 1000 degrees C into the epi. During the source/drain predep, phosphorous source wafers are used, resulting in a solid solubility limit of $1x10^{21}$ cm^{-3} (Ref 8:241). The diffusion coefficient for phosphorous, at 1000 degrees C and the above impurity doping concentration, is found to be $2.0175x10^{-13}$ cm^2-sec^{-1} (Ref 7:39).

Using this information, Table II-4 was compiled. Again, solving equation II-6 for Q, and substituting the value into equation II-5, equation II-5 was solved for the source/drain diffusion depth after the drive, and equation II-4 was solved for the source/drain diffusion depth after the source/drain predep.

This concluded the initial calculations for the

TABLE II-4

Initial Calculations for Source/Drain Diffusion

	D (cm^2-sec^{-1})	t (sec)	Dt (cm^2)	Σ Dt (cm^2)	x_j (μm)
Source/Drain Predep	2.0175×10^{-13}	900	1.8158×10^{-10}	1.8158×10^{-10}	.8626
Source/Drain Drive	"	1200	2.4210×10^{-10}	2.4210×10^{-10}	1.9146

$$N(x,t) = N_o(\text{erfc}(x_j 2^{-1}(Dt)^{-1/2}))$$

$$Q(t) = 2N_o(Dt)^{1/2}\pi^{-1/2}$$

$$= 1.5205 \times 10^{16}\ cm^{-2}$$

$$N(x,t) = Q(\pi Dt)^{-1/2}(\exp(-x_j^2(4Dt)^{-1}))$$

$$N_o = 1 \times 10^{21}\ cm^{-3}$$

$$N_b = 6 \times 10^{15}\ cm^{-3}$$

source/drain diffusion. The next step was to determine the thicknesses of the oxides required to mask all predeps and drives.

Calculating Oxide Mask Thicknesses

The use of a silicon dioxide layer serves two purposes: first, by selectivly etching the oxide, a pattern is formed through which impurities can diffuse into the wafer, and second, the oxide blocks, or masks, any diffusion from taking place outside the pattern area.

The use of silicon dioxide as a mask is highly effective as the diffusion coefficients for usual silicon dopants (boron, phosphorous) are several orders of magnitude lower in silicon dioxide than in silicon (Ref 8:210).

There are two oxide mask thicknesses that need to be determined. The first oxide must mask all three diffusions; isolation, gate, and source/drain. The second oxide, grown during the gate drive, must mask the source/drain diffusion.

The first oxide mask must be of a thickness that will mask boron for a total of 615 minutes at 1050 degrees C, and 35 minutes at 1000 degrees C. Since the difussion coefficient is higher for a higher temperature, the required minimum thickness was determined assuming the entire process is done at 1050 degrees C. At the same time, the first oxide must mask phosphorous for 35 minutes at 1000 degrees C. Approximately 0.3 microns of oxide are required to mask boron for 650 minutes at 1050 degrees C, and approximately

0.25 microns of oxide are required to mask phosphorous for 35 minutes at 1000 degrees C (Ref 7:231-232). Therefore, 0.3 microns of initial oxide should be sufficient to effectively mask the wafer for the entire process. To be on the safe side, however, approximately 0.5 microns of initial oxide would be grown.

The second oxide, over the isolation and gate diffusions, must be on the order of 0.25 microns, as previously shown, to mask the phosphorous. Again, to be on the safe side, 0.3 microns of gate oxide would be grown.

Finally, a third oxide needs to be grown during the source/drain drive. This oxide serves as a passivating layer and is not required to mask any diffusions. It should be on the order of .2 microns or more to prevent pinholing.

The method used to grow the necessary oxides was thermal oxidation of silicon through the following chemical reactions (Ref 7:22):

$$Si(solid) + O_2 \text{ yields } SiO_2(solid) \qquad \text{(II-7)}$$

$$Si(solid) + 2H_2O \text{ yields } SiO_2(solid) + 2H_2 \qquad \text{(II-8)}$$

Through these reactions, oxide is formed by consuming some of the silicon on which it grows. Approximately 45% of the oxide thickness comes from the silicon surface (Ref 7:23).

Equation II-8 yields a much faster oxide growth than equation II-7. However, equation II-7 has been shown to

produce a rapid initial phase of oxidation amounting to about 0.02 microns, where this initial rapid growth has not been observed in equation II-8 (Ref 7:31). Therefore, when possible, an oxide is started in dry O_2 to obtain the rapid initial phase, while a subsequent switch to wet O_2 (steam) rapidly grows the oxide to the desired thickness.

Table II-5 shows the various times required to grow the necessary oxide thicknesses, starting with dry O_2, switching over to wet O_2, and then switching back to dry O_2 again. The second dry O_2 stage helps to anneal and densify the oxide (Ref 8: 229-230).

Pictoral Summary of Chapter II

Using the final diffusion results from the previous tables, and taking into account the amount of silicon lost through oxide growth, a cross-section of the wafer is depicted in Figure 1. This figure shows the relationship between the epi, isolation, gate, source/drain, and oxides as they would appear according to the calculations of this chapter.

TABLE II-5

Oxide Growth Calculations

Time	Temperature	Condition	Oxide
	Initial Oxide		
20.0 min	1050 degrees C	Dry O_2	500 angstroms
48.5 min	1050 degrees C	Wet O_2	4500 angstroms
20.0 min	1050 degrees C	Dry O_2	neglible
		TOTAL	5000 angstroms
	Gate Oxide		
20.0 min	1050 degrees C	Dry O_2	500 angstroms
19.8 min	1050 degrees C	Wet O_2	2500 angstroms
20.0 min	1050 degrees C	Dry O_2	neglible
		TOTAL	3000 angstroms
	Source/Drain Oxide		
20.0 min	1000 degrees C	Dry O_2	300 angstroms
16.8 min	1000 degrees C	Wet O_2	1700 angstroms
20.0 min	1000 degrees C	Dry O_2	minimal
		TOTAL	2000 angstroms

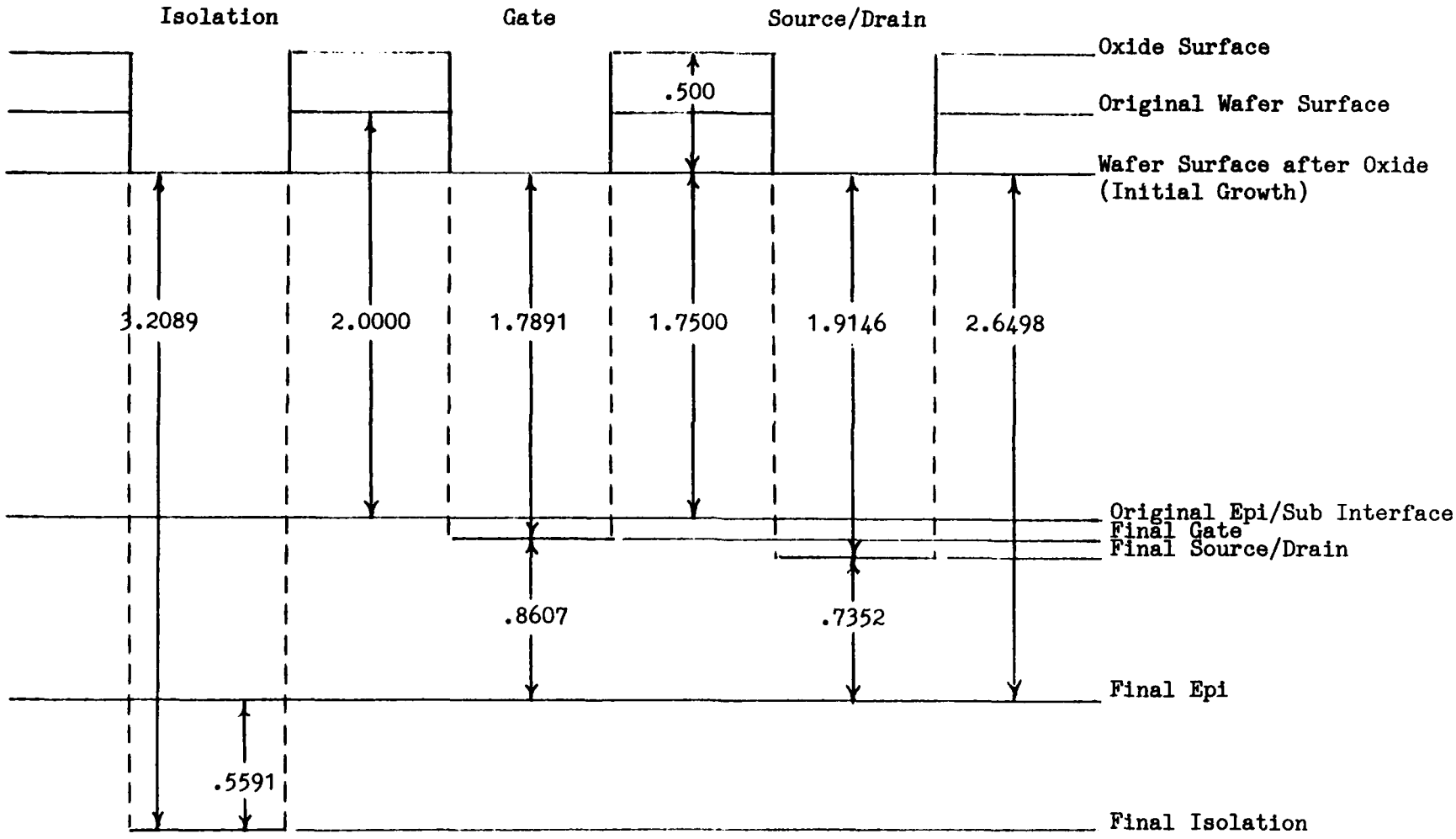

Figure II-1. Cross-sectional depiction of diffusion depths relative to each other.

CHAPTER III

JFET FABRICATION

Introduction

Before actually fabricating the JFET array, several test processes were required. These test processes included: Growing initial oxides to check the oxidation tube operation; growing more oxides to check the cleanliness quality of the grown oxides through C-V testing; performing a test boron diffusion to check the operation of the p-type tube, and to check the deposition properties of the boron source wafers; and, finally, performing a test phosphorous diffusion to check the operation of the n-type tube, and to check the deposition properties of the phosphorous source wafers.

After the test processes, the actual circuit wafer steps were performed. These steps include: Growing the initial mask oxide, processing the isolation mask, processing the gate mask, processing the source/drain mask, processing the contact window mask, and processing the metallization mask.

Growing Test Oxides

Having profiled the diffusion furnace (see Appendix E), several additional setup steps were accomplished. First, the N_2 and O_2 gas flows to all three tubes were adjusted to one liter per minute and one atmosphere of pressure. Next,

the steam bubbler controller was adjusted until the bubbler temperature was between 95 and 100 degrees C. Finally, the three sets of gas flow timers were functionally checked to insure they cycled properly. Timer 1 controls the time for the first stage of dry O_2, timer 2 controls the time for the wet O_2, and timer 3 controls the time for the second stage of dry O_2. If no timers are running, the tubes are continually being purged with dry N_2. The timers and bubbler operated properly, indicating the furnace tubes and associated controls were ready for use.

Three, three inch test wafers were cleaned, using cleaning/etching solution CL1 (see Appendix B), and placed, individually, in the furnace to grow oxides. The first wafer was to have 5000 angstroms grown on it, the second wafer was to have 2000 angstroms grown on it, and the third wafer was to have 1000 angstroms grown on it. Since 1000 angstroms was not included in Table II-5 calculations, the time required to grow 1000 angstroms was calculated, and Table III-1 compiled to reflect the three oxide growths (Ref 8: 229-230).

The wafers used to grow the initial test oxides were: Microwave Associates Inc., 3.8-4.2 microns n-type epi with a resistivity of one ohm-cm, on a p-type substrate. These wafers produce slightly different results than obtained with other types of wafers, but, the differences are small enough not to cause significant deviations between types of wafers.

TABLE III-1

Test Oxide Growth Calculations

Time	Temperature	Condition	Oxide
	5000 Angstroms		
20.0 min	1050 degrees C	Dry O_2	500 angstroms
48.5 min	1050 degrees C	Wet O_2	4500 angstroms
20.0 min	1050 degrees C	Dry O_2	negligible
	2000 Angstroms		
20.0 min	1050 degrees C	Dry O_2	500 angstroms
19.8 min	1050 degrees C	Wet O_2	1500 angstroms
20.0 min	1050 degrees C	Dry O_2	negligible
	1000 angstroms		
20.0 min	1050 degrees C	Dry O_2	500 angstroms
4.2 min	1050 degrees C	Wet O_2	500 angstroms
20.0 min	1050 degrees C	Dry O_2	minimal

One aspect of introducing the wafers into the furnace was investigated during this initial oxide growth. How fast could the wafers go from room temperature to furnace temperature ("pushing"), and vice-versa ("pulling"), without damage to the wafers. This was an important aspect in that "pushing" or "pulling" the wafers too fast could thermally stress them enough to cause warping, or even breaking. If the warping is severe enough, proper exposure could not be

obtained during photolithographic processing (see Appendix C). On the other hand, it seemed apparent that "pushing" or "pulling" too slow would introduce significant deviations in all furnace processes by reducing the actual time at the temperature specified in the process calculations.

While previous fabrications had used push/pull rates of two inches per minute, a much faster rate sould give more accurate results, if the wafers could withstand the thermal stresses. To test the wafer's ability to withstand these stresses, the first test wafer was placed into the tube opening, and immediately pushed to the center (49.5 inches) at a two feet per minute rate. After growing the oxide, the wafer was pulled from the furnace at the same rate, with no apparent problems being observed. The second wafer was then placed into the tube opening, and immediately pushed the first two feet at the two feet per minute rate, and then pushed the remaining two feet in about five seconds. This second wafer was then withdrawn from the tube at the rate of the first two feet in about five seconds, and the last two feet at the two feet per minute rate. Again, no problems with warping or breaking occurred. Wafer three was then cycled at the same rate as the second wafer with satisfactory results. It should be noted that the times to push and pull the wafers are included in the total processing time.

Apparently, the majority of the stressing occured upon initially placing the wafers in the tube, and the first two

minutes allowed them to reach furnace temperature at a uniform enough rate that they suffered no effects from the subsequent rapid push to the center. Also, the last two minutes of pulling allowed the wafers to cool enough that suddenly subjecting them to room temperature did not stress them to an excess.

When each test wafer had completed the necessary oxide growth cycle, the oxide thicknesses were checked with an ellipsometer. Following the ellipsometer manufacturer's operating instructions (Ref 9, 10), the three oxide thicknesses were calculated to be: 4690 angstroms on the first wafer, 1550 angstroms on the second wafer, and 1040 angstroms on the third wafer. The first wafer's oxide measured as being almost 94 percent of the calculated thickness, and the third wafer's oxide measured as being a little over 100 percent of the calculated thickness. The second wafer's oxide, however, only measured about 77.5 percent of the calculated thickness, which was too much of a deviation. Upon rechecking the calculations and oxide growth charts, an error was discovered. The error had been made in reading the wet O_2 chart, and the time used in Tables II-5 and III-1, should have grown about 1500 angstroms of oxide. This brought all three test oxides within 90 percent of the expected, and indicated the oxide tube was functioning properly.

Having verified the oxidation tube operation, the next step was to grow different oxide thicknesses on some

additional wafers, and then check the quality of the oxide through capacitance-voltage (C-V) testing.

Measuring Oxide Quality by C-V Testing

The purpose of performing C-V tests was to check the "cleanliness" or "dirtiness" of a grown oxide. The measure of cleanliness is the number of mobile sodium ions present in the oxide. These undesirable ions can be introduced by various means, but primarily they are introduced through the use of "dirty" furnace tubes. As the tubes are heated to processing temperatures, sodium ions diffuse out of the quartz walls and contaminate the oxide as it grows.

One means of reducing this contamination is to etch the inside of the tubes with gaseous hydrochloric acid prior to growing the oxides. Having etched the tubes, chlorine ions diffuse out of the tube walls during oxide growth, bind with the sodium ions, and produce electrically neutral sodium-chloride molecules. However, in this thesis project, this initial etch was not performed, because the equipment required to dispose of the gaseous hydrochloric acid was not available.

In order to perform the C-V tests, oxide was grown on four test wafers. The test wafers were: SCI, Silicon Material Division, 4.0-4.5 microns n-type epi with a resistivity of 1.0-1.1 ohm-cm, on a 15 mils n-type substrate with a resistivity of .005 ohm-cm. This configuration eliminates the p-n junction diode that could result in

erroneous readings during C-V plotting.

Again, the first wafer required 5000 angstroms of oxide grown on it, the second wafer required 2000 angstroms of oxide grown on it, and the third and fourth wafers required 1000 angstroms of oxide grown on each. These oxide thicknesses were then checked with the ellipsometer with the following results. The first wafer's oxide calculated to be 4920 angstroms, the second wafer's oxide calculated to be 2260 angstroms, and both the third and fourth wafer's oxides calculated to be 1610 angstroms.

At this point, being totally confused as to why the actual grown oxides did not match the calculated, the times to grow 5000, 3000, 2000, and 1000 angstroms of oxide were refigured. Apparently, sometimes the dry O_2 growth was not taken into account when reading the wet O_2 chart. Making doubly sure that the charts were read properly this time, Table III-2 was compiled showing the corrected times required for all four oxides.

The next step to be performed was the deposition of an aluminum dot pattern over the entire oxide surface. To do this, the wafers were placed in a vacuum vapor deposition chamber with a stainless steel mask containing a matrix of holes 40 mils in diameter on 50 mils centers. The vacuum vapor deposition chamber was prepared according to the manufacturer's operating instructions (Ref 11, 12), and the desired dot pattern was made. These aluminum dots were needed to insure good electrical contact with the oxide when

performing the C-V tests.

TABLE III-2

Revised Oxide Growth Calculations

Time	Temperature	Condition	Oxide
	5000 Angstroms		
20.0 min	1050 degrees C	Dry O_2	500 angstroms
48.6 min	1050 degrees C	Wet O_2	4500 angstroms
20.0 min	1050 degrees C	Dry O_2	negligible
	3000 Angstroms		
20.0 min	1050 degrees C	Dry O_2	500 angstroms
17.4 min	1050 degrees C	Wet O_2	2500 angstroms
20.0 min	1050 degrees C	Dry O_2	negligible
	2000 Angstroms		
20.0 min	1000 degrees C	Dry O_2	300 angstroms
14.3 min	1000 degrees C	Wet O_2	1700 angstroms
20.0 min	1000 degrees C	Dry O_2	negligible
	1000 Angstroms		
20.0 min	1050 degrees C	Dry O_2	500 angstroms
2.4 min	1050 degrees C	Wet O_2	500 angstroms
20.0 min	1050 degrees C	Dry O_2	minimal

The following is one method of evaluating the presence

of mobile sodium ions in silicon dioxide. First the C-V is measured at room temperature. Next, with an applied 10 volt dc bias per 1000 angstroms of oxide, the wafer is heated to 150-300 degrees C for one minute to three hours, thus causing the mobile ions to drift due to the influence of the electrical field bias. Finally, the dc bias is removed, and the C-V is again measured (Refs 13:49-56; 14:46-55).

If the oxides are "clean", there will be approximately 10^{10} to 10^{11} charges per cm^2, whereas a "dirty" oxide will have between 10^{11} and 10^{14} charges per cm^2. Approximately 10^{11} charges per cm^2 are drifted for each one volt of shift for an oxide 2000 angstroms thick. This drift is a linear relationship in that two volts for an oxide 4000 angstroms thick will produce the same result. It is possible to achieve $2x10^{10}$ charges per cm^2 drift for an oxide thickness of 1000 angstroms, resulting in a 0.1 volt, or less, shift after applying BT, where:

B = $2x10^6$ volt-cm^{-1} of oxide thickness

T = 300 degrees C for five minutes

Applying a positive BT causes the resulting plotted curve to shift to the left (-). For a given BT, the dirtier the oxide, the greater the shift (Ref 13:49-56; 14:46-55; 15:657-670).

Having measured the oxide thickness, the capacitance of the oxide can be calculated using the equation:

$$C = \epsilon_o \epsilon_r A d^{-1} \qquad \text{(III-1)}$$

where

C is capacitance,

$\epsilon_o = 8.854 \times 10^{-12}$ F-m^{-1}, is the permittivity of free space,

$\epsilon_r = 3.9$, is the dielectric constant of silicon dioxide, and

$A = 8.11 \times 10^{-7}$ m^2, is the area of the aluminum dot.

For the first wafer, the thickness of the oxide was $.4920 \times 10^{-6}$ m. Substituting into equation III-1 gave a capacitance of 56.9pf. For the second wafer, the thickness of the oxide was $.2260 \times 10^{-6}$ m. Substituting into equation III-1 gave a capacitance of 124pf. Finally, for the third and fourth wafers, the thickness of the oxide was $.1610 \times 10^{-6}$ m. Substituting into equation III-1 gave a capacitance of 174pf.

Next, the C-V tests were performed on the four wafers, using the information available for the C-V Plotter (Ref 16). A positive 25 volt dc bias was applied to each wafer, and the ramp start and stop voltages set to +10 volts and -40 volts respectively. A C-V plot was then obtained at room temperature. Each wafer was then heated to 220 degrees C for five minutes with the bias applied, and another C-V plot was obtained. The results of a typical C-V plot are

shown in Figure III-1.

From two wafers, in which there was complete confidence in the data, the mobile ion presence was concluded to be 3-4 x 10^{11} cm^{-2}. These numbers of mobile ions are slightly higher than what constitutes a "clean" oxide, however, the numbers are low enough that they should not cause significant problems in the completed circuits.

Having verified the oxidation tube operation, and checked the C-V characteristics of the grown oxides, the next step was to perform a boron test diffusion.

Testing Boron Predep

A boron test diffusion was required to verify proper p-tube operation, and to check the surface resisitivity of the boron predep against data supplied by the boron source manufacturer. The boron source wafers used were: Planar Diffusion Sources, Boron Nitride, Grade BN-1100 manufactured by PDS, Graphite Products Division, Carborundum Co. The silicon wafers used were the same type used to perform the C-V tests.

Four test wafers were cleaned using cleaning/etching solution CL1, placed in a "boat" with the boron diffusion sources, and pushed to the center of the p-tube for a 20 minute predep at 1050 degrees C. After the predep, the borosilicate glass which formed during the predep was removed using cleaning/etching solution CL2, and the surface resistivity of each wafer was measured with a four-point

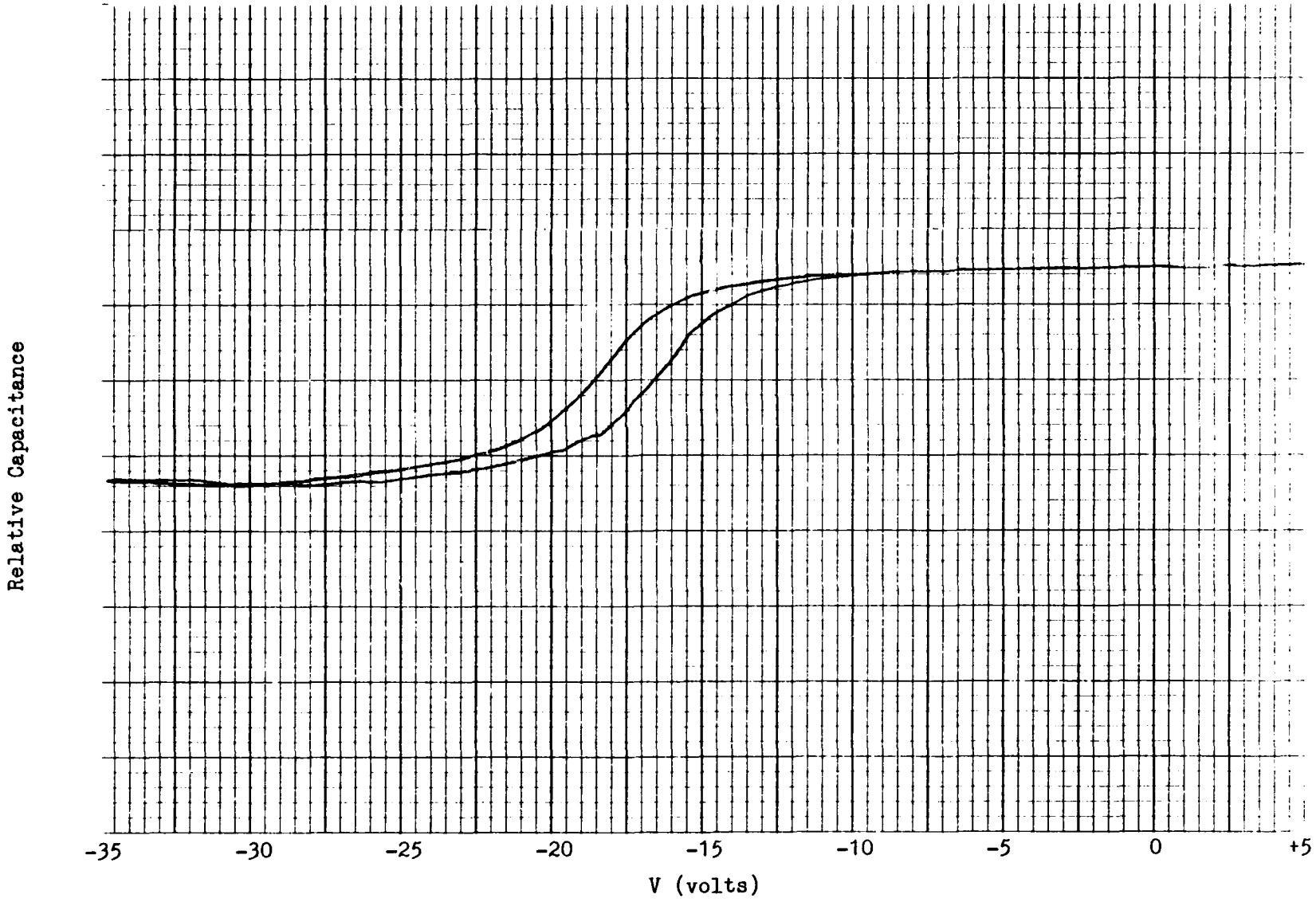

Figure III-1. Typical C-V Plot Results.

probe. The four-point probe was set up according to the manufacturer's operating instructions (Ref 17) and each wafer probed in five different positions. The average surface resistivity of each wafer was then calculated.

Next, the wafers were surface cleaned using cleaning/etching solution CL3, and placed in the furnace, without the source wafers, to accomplish the diffusion drive. After the drive, a four-point probe was performed on the wafers, and the average surface resistivity again calculated. The two sets of average resistivity calculations are shown in Table III-3 below.

TABLE III-3

Average Boron Surface Resistivity

Wafer 1	Wafer 2	Wafer 3	Wafer 4
	After Predep		
15.33	15.46	16.07	17.05
	After Drive		
17.00	17.19	17.77	19.01

The average resistivity of the boron predep followed very closely to the manufacturer's specified predep resistivity of 14 ohms per square at 1050 degrees C for 20 minutes (Ref 18). It was noted that wafer one, being closest to the gas source, had the lowest surface

resistivity, while wafer four, being the farthest from the gas source had the highest. This might possibly have resulted from the gas swirling in the tube, disturbing the flow of atoms from the source wafer to the silicon wafers and producing a non-uniform deposition.

It appeared the p-tube was operating properly, so the next step was to operationally check the n-tube by performing a test phosphorous diffusion.

Testing Phosphorous Predep

As with the boron test diffusion, a phosphorous test diffusion was required to verify proper furnace operation, and to check the surface resistivity of the phosphorous predep against data supplied by the phosphorous source manufacturer. The phosphorous source wafers used were: Planar Diffusion Sources, Phosphorous, Grade PH-1000 manufactured by PDS, Graphite Products Division, Carborundum Co. The silicon wafers used were the same wafers used for the test boron diffusion.

The four wafers were surface cleaned using cleaning/etching solution CL3, placed in a "boat" with the phosphorous diffusion sources, and pushed to the center of the n-tube for a 20 minute predep at 1000 degrees C. After the predep, the four-point probe was used to measure the surface resistivity of the wafers. Each wafer was probed in five positions, and the average resistivity of each wafer calculated.

Next, the wafers were surface cleaned with cleaning/etching solution CL3, and placed back in the furnace, without the source wafers, to accomplish the diffusion drive. After the drive, a four-point probe was performed, and the average resistivity again calculated. The two sets of average resistivity calculations are shown in Table III-4 below.

TABLE III-4

Average Phosphorous Surface Resistivity

Wafer 1	Wafer 2	Wafer 3	Wafer 4
	After Predep		
6.94	6.79	6.86	7.25
	After Drive		
4.86	4.66	4.60	4.64

The average resistivity of the phosphorous predep followed very closely to the manufacturer's specified predep resistivity of 8 ohms per square at 1000 degrees C for 20 minutes (Ref 19). While it appeared the predep resistivity almost followed the same pattern as noted for the boron, lower resistivity at the gas source and higher resitivity farther away, it is not known why the resistivity after the drive was essentially reversed.

Having concluded the test diffusions, the actual

circuit wafer fabrication processes could now be performed.

Growing JFET Wafer Oxides

The silicon wafers used for circuit fabrication were: Microwave Associates Inc., 2 microns n-type epi with a resistivity of .9 ohm-cm on a 20 mils p-type (100) substrate with a resistivity of 40 ohm-cm. Fourteen of these wafers were cleaned using cleaning/etching solution CL1, positioned in a "boat", and then placed in the furnace oxidation tube to grow 5000 angstroms of oxide per the information for oxide growth in Table III-2.

After growing the necessary oxides, the first and last wafers in the boat were checked with an ellipsometer to verify the oxide thicknesses. At this point, only the two wafers were checked in order to reduce the possibility of contaminating the wafers through excessive handling. The first wafer (closest to the steam source) measured 4545 angstroms, and the last wafer (farthest from the steam source) measured 4385 angstroms. While these oxides were less than the anticipated 5000 angstroms, the oxides were sufficient to mask all the required diffusions. Therefore, the wafers were not placed back in the furnace to grow more oxide. The oxide thicknesses of the other wafers should fall within the measured range of the first and last wafers.

Having grown the initial oxides, eight of the fourteen wafers were selected for processing. These eight wafers included six circuit wafers, which hopefully would produce

working devices, plus two test wafers. The purpose of the test wafers was to permit checking the diffusion depths as the fabrication proceeded and thereby make any necessary corrections in the diffusion processes. The first process was the isolation diffusion.

Diffusing JFET Isolation

The isolation diffusion process involved the isolation mask photolithography process, etching of the isolation pattern, and the isolation diffusion. The actual isolation diffusion was a p-type (boron) diffusion that was driven through the n-type epi into the p-type substrate, thus forming a "well" of n-type material in which the JFET was made. Isolation was achieved by virture of a reversed-biased p-n junction totally surrounding each JFET, and thereby isolating it from all adjacent JFETs.

The isolation mask was positioned in the mask aligner, the mask aligner was set up according to the manufacturer's operating instructions (Ref 20), and the eight wafers were surface cleaned using cleaning/etching solution CL3. The wafers were then processed using the photolithography procedures outlined in Appendix C. Several photolithographic iterations were done on each wafer before acceptable patterns were obtained; somewhat due to the fine geometries of the isolation mask (5 microns), but also because of undersirable dust on the wafers and mask.

Even though each wafer was blown off several times,

dust would still settle on the wafer surface. At the least, the dust would cause an opening in the pattern, by blocking the light and thereby not exposing a small area of photoresist(PR). Usually though, the dust stuck to the mask, necessitating repeated scrubbings.

Next, the oxide patterns were etched using the procedures outlined in Appendix D, with one observed peculiarity. Upon microscopic inpection, some of the patterns appeared very ragged. There was, however, some pattern to the raggedness. Apparently, even though the wafers looked clean, not all the PR or adhesion promoter had been removed between successive exposures and the resulting film had somehow retained the image of the previous exposure. Even though the developed patterns looked all right, after etching, the patterns looked like greatly misaligned double exposures. The double image only appeared where the lines of a previous exposure crossed the lines of a subsequent exposure. Increasing the PR removal time to about 10 seconds precluded this peculiarity from appearing in later processes.

After etching, a 40 minute boron predep was performed, followed by a 6 hour and 40 minute drive. Each wafer was then four-point probed, and the average surface resistivity of each wafer calculated. These figures are shown in Table III-5.

Actually, not much can be inferred from this data as in most cases the measurements had to be taken between

one-eighth and one-fourth of an inch from the edge of the wafer, due to the field oxide covering most of the wafer surface. This small area around the edge of the wafers does not receive the same amount of dopant, during the predep, as does the rest of the wafer. This decrease in dopant is a function of the source wafers, and cannot be compensated for.

TABLE III-5

Post Isolation Drive Resistivity

Wafer 1	Wafer 2	Wafer 3	Wafer 4
6.30	7.76	8.65	11.72
Wafer 5	**Wafer 6**	**Wafer 7**	**Wafer 8**
6.92	7.67	8.20	8.10

After the isloation process was completed, there appeared to be "bubbles" in the isolation diffusion lines as seen in Figure III-2. Suspecting it may have been some borosilicate glass that had not been removed, the first wafer was recleaned and reexamined. The bubbles were still there, so the entire oxide layer was etched away to see if the bubbles would disappear, but they did not. However, no bubbles were noted in later processes.

Next, two small chips from wafer one were beveled and stained to check the epi layer and isolation diffused depths. The first chip was taken from an area that had been

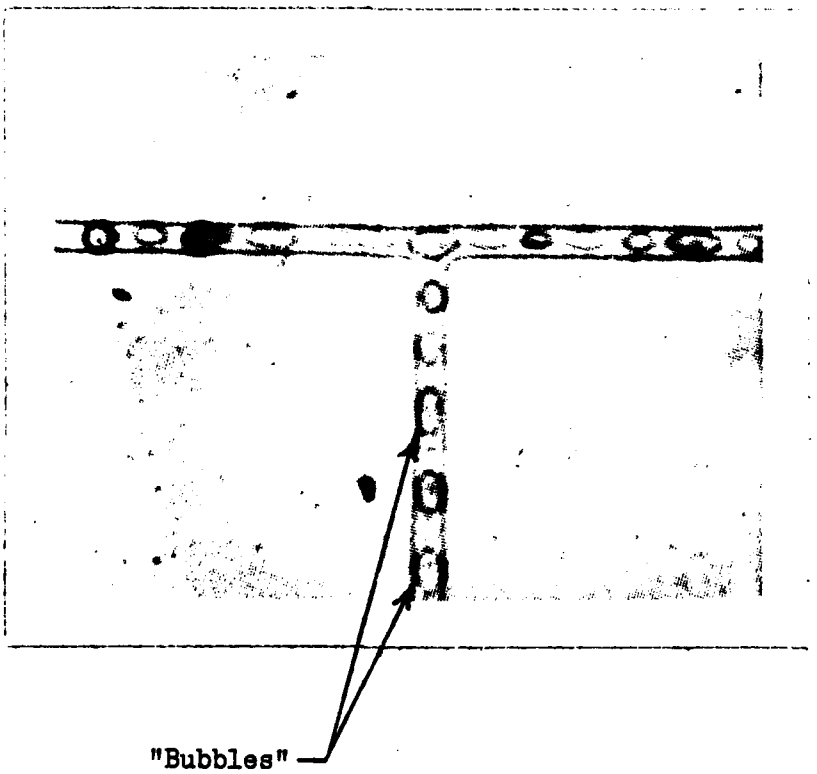

Figure III-2. Isolation Diffusion Anomaly.

covered by oxide during the isolation predep and drive, and was used to check the epi. The other chip was taken from an area that had been free of any oxide and therefore had the boron diffused into the wafer.

Each wafer was then checked under an interferometer, and pictures were taken to determine the depths. The interferometer causes fringing lines to appear that can be rotated until they are perpendicular to the edge of the bevel. As the lines cross the bevel, they drop off at an angle. Each fringe line is equal to 2700 angstroms, so by counting the number of fringe lines crossing the area of interest, the width of that area can be measured.

The first photograph, shown in Figure III-3, is the isolation after the isolation diffusion drive. By closely examining the photograph, 12.5 lines were counted crossing the dark stained area, implying the isolation diffused to a depth of 3.375 microns. The second photograph, shown in Figure III-4, is the epi after the isolation drive. By closely examining this photograph, 8.5 lines were counted crossing the light band, implying the epi had diffused to a total depth of 2.295 microns. This means the isolation diffusion overran the epi by 1.080 microns, and thereby insured isolation. These depths, however, did not correspond to the predicted values obtained in Chapter II. Therefore, a new set of tables had to be derived.

The problem with the tables in Chapter II is that the diffusion coefficients obtained from Grove were off

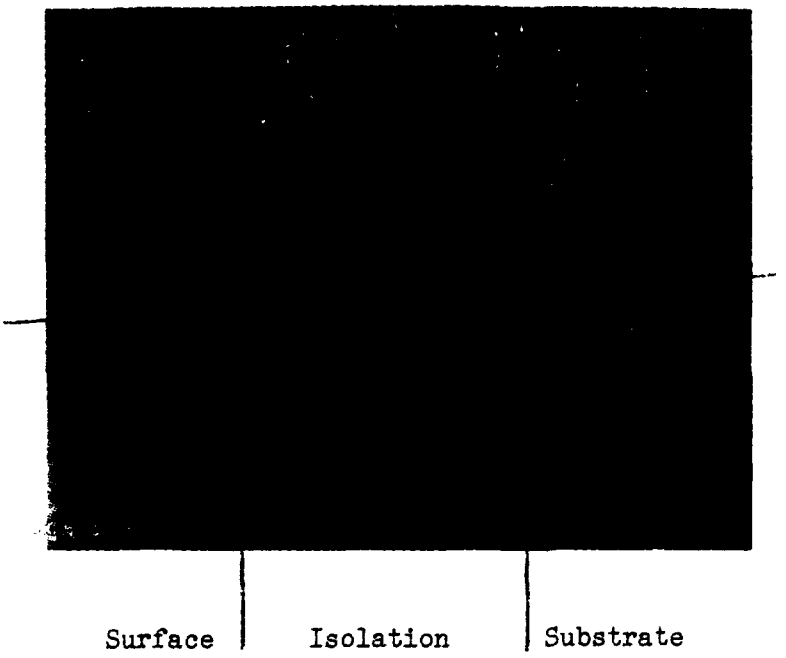

Figure III-3. Bevel and Stain of Isolation Diffusion After Isolation Drive.

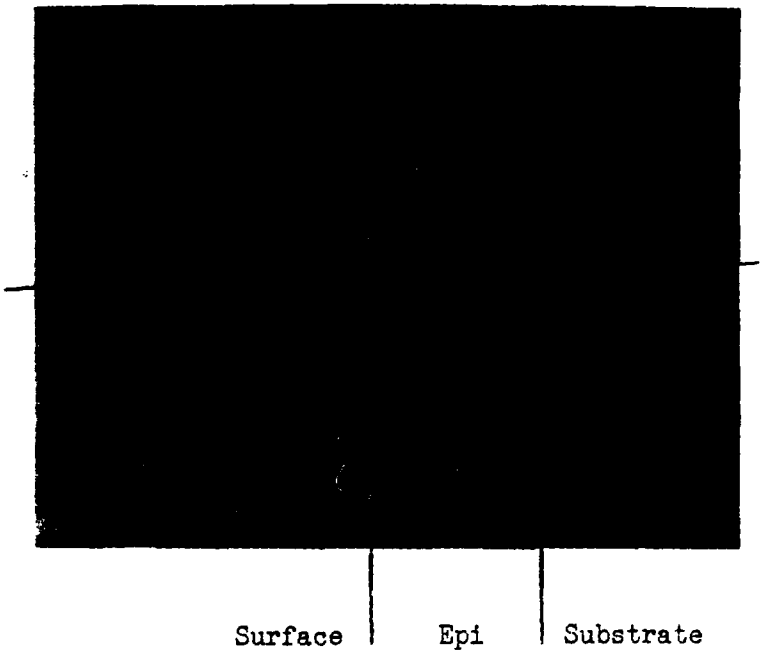

Figure III-4. Bevel and Stain of Epi-Layer After Isolation Drive.

considerably. Constructing the new tables required correcting the diffusion coefficients for both boron and phosphorous. Computing the new diffusion coefficient for phosphorous required calculating how far the epi diffused during the processes (it started out at 2 microns). Assuming the wafers grew .5 microns of oxide, and that 50% of the oxide thickness came from the silicon, then .25 microns of epi were lost to oxide, leaving 1.75 microns of original epi. The actual diffused depth then is the difference between the measured depth, and the original depth, or .545 microns. Recalling equation II-2, and substituting the .545 microns for x_j and solving for D, the diffusion coefficient of phosphorous at 1050 degrees C was found to be 2.4478×10^{-14} $cm^2\text{-}sec^{-1}$. Using the ratio of the new diffusion coefficient to the old diffusion coefficient and finding the percentage of error, the diffusion coefficient of phosphorous at 1000 degrees C was determined to be 7.2614×10^{-15} $cm^2\text{-}sec^{-1}$.

Finding the new diffusion coefficient for boron was not quite as simple. The actual isolation diffused depth was 3.375 microns, however, this was obtained through a combination of erfc and gaussian diffusions. Therefore, recalling equations II-4, -5, and -6, and iteratively picking a diffusion coefficient and substituting into the equations, the boron diffusion coefficient at 1050 degrees C was found to be 7.2315×10^{-14} $cm^2\text{-}sec^{-1}$. Using the ratio of old to new and finding the percentage of error, the

diffusion coefficient of boron at 1000 degrees was determined to be 2.1452×10^{-14} cm^2-sec^{-1}.

Using these new diffusion coefficients, the data in Tables II-1, -2, -3, and -4 were recompiled. It became apparent that because the boron diffused faster and the phosphorous diffused slower than previously predicted, the gate drive needed to be shortened considerably in order to prevent driving the gate through the epi and shorting out the gate. Making all the necessary changes in the data, Tables III-6, -7, -8, and -9 were constructed. Also a new cross-sectional depiction was made, and is shown in Figure III-5.

Having completed the isolation diffusion, the next step was to perform the gate diffusion.

Diffusing JFET Gate

The gate diffusion process involved the gate mask photolithography process, the etching of the gate pattern, and the gate diffusion. The actual diffusion is another p-type diffusion into the epi.

The gate mask was positioned in the mask aligner, and the seven wafers surface cleaned using cleaning/etching solution CL3. The wafers were then processed using the photolithography procedures outlined in Appendix C. Since the gate geometries were somewhat bigger than the isolation geometries, sufficient patterns were obtained with only 10 second exposure and 35 second developing times.

TABLE III-6

Revised Calculations for Epi Diffusion

	D (cm^2-sec^{-1})	t (sec)	Dt (cm^2)	Σ Dt (cm^2)	x_j (μm)
Initial Oxide	2.4478×10^{-14}	5316	1.3013×10^{-10}	1.3013×10^{-10}	.2231
Isolation Predep	"	2400	5.8747×10^{-11}	1.8888×10^{-10}	.2688
Isolation Drive	"	24000	5.8747×10^{-10}	7.7635×10^{-10}	.5450
Gate Predep	"	900	2.2030×10^{-11}	7.9838×10^{-10}	.5527
Gate Drive	"	5400	1.3218×10^{-10}	9.3056×10^{-10}	.5967
Source/Drain Predep	7.2614×10^{-15}	900	6.5353×10^{-12}	9.3709×10^{-10}	.5988
Source/Drain Drive	"	1200	8.7137×10^{-12}	9.4581×10^{-10}	.6015

$$N(x,t) = N_s 2^{-1}(\text{erfc}(x_j 2^{-1}(Dt)^{-1/2}))$$

$$N_s = 6 \times 10^{15}\ cm^{-3}$$

$$N_b = 5 \times 10^{14}\ cm^{-3}$$

TABLE III-7

Revised Calculations for Isolation Diffusion

	D (cm^2-sec^{-1})	t (sec)	Dt (cm^2)	Σ Dt (cm^2)	x_j (μm)
Isolation Predep	7.2315×10^{-14}	2400	1.7356×10^{-10}	1.7356×10^{-10}	.8065
Isolation Drive	"	24000	1.7356×10^{-9}	1.7356×10^{-9}	3.3752
Gate Predep	"	900	6.5084×10^{-11}	1.8007×10^{-9}	3.4204
Gate Drive	"	5400	3.9050×10^{-10}	2.1912×10^{-9}	3.6750
Source/Drain Predep	2.1452×10^{-14}	900	1.9307×10^{-11}	2.2105×10^{-9}	3.6870
Source/Drain Drive	"	1200	2.5742×10^{-11}	2.2362×10^{-9}	3.7028

$$N(x,t) = N_o(\text{erfc}(x_j 2^{-1}(Dt)^{-1/2}))$$

$$Q(t) = 2N_o(Dt)^{1/2}\pi^{-1/2}$$

$$= 5.9462 \times 10^{15}\ cm^{-2}$$

$$N(x,t) = Q(\pi Dt)^{-1/2}(\exp(-x_j^2(4Dt)^{-1}))$$

$$N_o = 4 \times 10^{20}\ cm^{-3}$$

$$N_b = 6 \times 10^{15}\ cm^{-3}$$

TABLE III-8

Revised Calculations for Gate Diffusion

	D (cm^2-sec^{-1})	t (sec)	Dt (cm^2)	Σ Dt (cm^2)	x_j (μm)
Gate Predep	7.2315×10^{-14}	900	6.5084×10^{-11}	6.5084×10^{-11}	.4939
Gate Drive	"	5400	3.9050×10^{-10}	3.9050×10^{-10}	1.7286
Source/Drain Predep	2.1452×10^{-14}	900	1.9307×10^{-11}	4.0981×10^{-10}	1.7572
Source/Drain Drive	"	1200	2.5742×10^{-11}	4.3555×10^{-10}	1.7942

$$N(x,t) = N_o(\text{erfc}(x_j 2^{-1}(Dt)^{-1/2}))$$

$$Q(t) = 2N_o(Dt)^{1/2}\pi^{-1/2}$$

$$= 3.6413 \times 10^{15}\ cm^{-2}$$

$$N(x,t) = Q(\pi Dt)^{-1/2}(\exp(-x_j^2(4Dt)^{-1}))$$

$$N_o = 4 \times 10^{20}\ cm^{-3}$$

$$N_b = 6 \times 10^{15}\ cm^{-3}$$

TABLE III-9

Revised Calculations for Source/Drain Diffusion

	D (cm^2-sec^{-1})	t (sec)	Dt (cm^2)	Σ Dt (cm^2)	x_j (μm)
Source/Drain Predep	2.0175×10^{-13}	900	1.8158×10^{-10}	1.8158×10^{-10}	.8626
Source/Drain Drive	"	1200	2.4210×10^{-10}	2.4210×10^{-10}	1.9146

$$N(x,t) = N_o(\text{erfc}(x_j 2^{-1}(Dt)^{-1/2}))$$

$$Q(t) = 2N_o(Dt)^{1/2}\pi^{-1/2}$$

$$= 1.5205 \times 10^{16}\ cm^{-2}$$

$$N(x,t) = Q(\pi Dt)^{-1/2}(\exp(-x_j^2(4Dt)^{-1}))$$

$$N_o = 1 \times 10^{21}\ cm^{-3}$$

$$N_b = 6 \times 10^{15}\ cm^{-3}$$

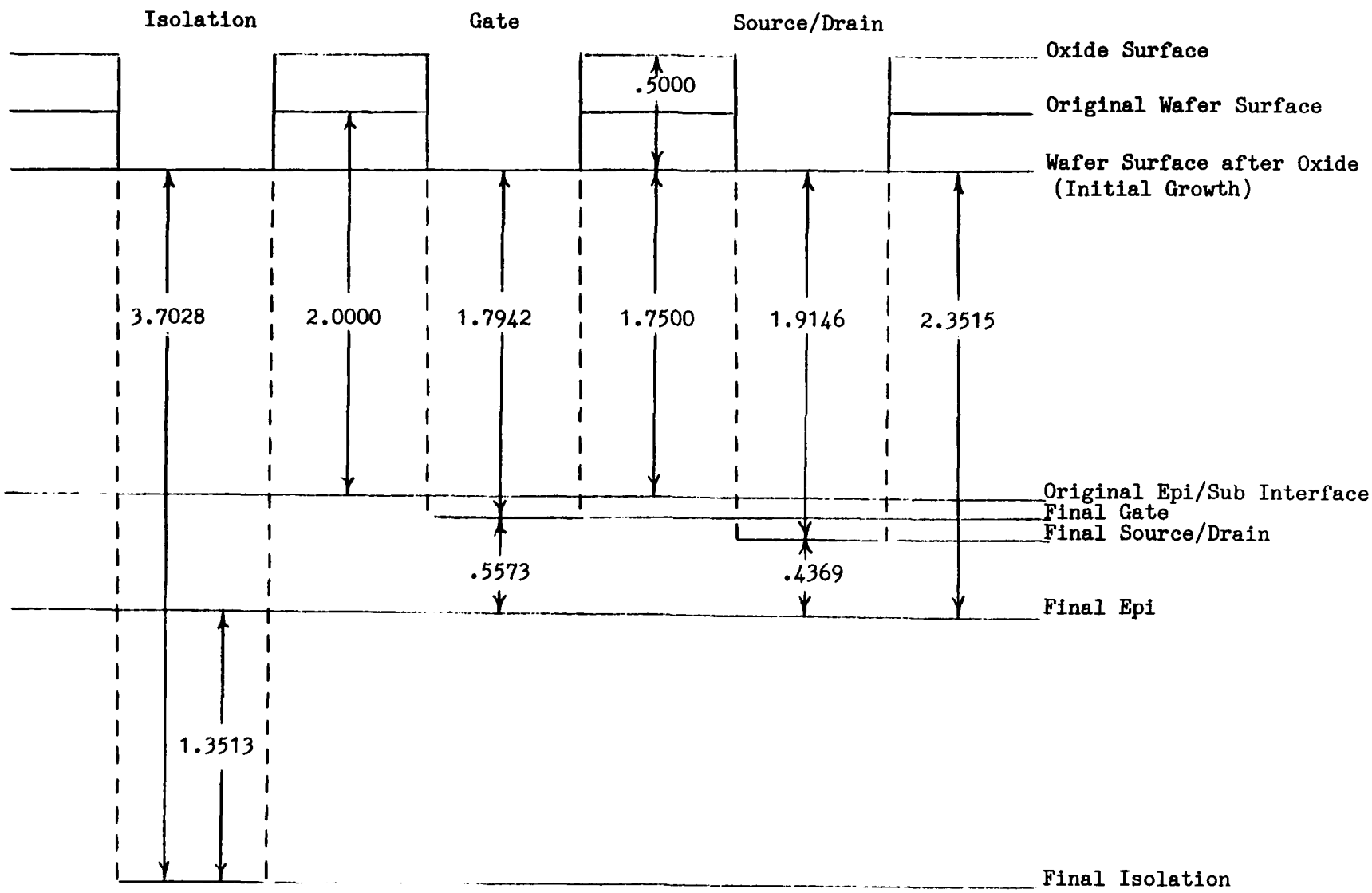

Figure III-5. Revised cross-sectional depitction of diffusion depths relative to each other.

During the exposure step of the photolithographic process, wafer six was broken when the mask aligner chuck jammed inside the machine during the automatic rotation that occurs after exposing the wafer. This wafer could not be used in subsequent mask aligner operations. However, it was processed along with the rest of the wafers in the diffusion processes, and was used as a test wafer for bevel and stain.

After developing the wafers, and inspecting them under the microscope, the field oxides were noted to be of a considerably different color than the color of the oxide after if was first grown. The wafers were checked with the ellipsometer and the calculated oxide thicknesses shown in Table III-10.

TABLE III-10

Pre-Gate Field Oxide Thicknesses

Wafer 1	Wafer 2	Wafer 3	Wafer 4
-	2000	2100	2180
Wafer 5	**Wafer 6**	**Wafer 7**	**Wafer 8**
2500	-	1760	1860

These thicknesses seemed low, so the color of the oxide was cross-checked against an oxide color chart. The oxide thicknesses determined by both the ellipsometer and color chart methods agreed. The final test would be in the pattern etching.

Feeling certain the oxides were as thin as indicated, they were only etched one minute and then checked under the microscope. All patterns, except those of wafer 5, etched clean in just over one minute, where wafer 5 etched clean in about one and one-half minutes. Inadvertantly, the cleaning/etching solution CL4 had been mixed 5:1 instead of 6:1, thereby producing an etch rate of about 1600 angstroms per minute. This was final proof that the oxides were as thin as indicated.

Checking the text by Glaser, showed that the oxide available should be just enough to mask a boron diffusion during the remaining 2.3 hours diffusion time, assuming the entire time would be at 1050 degrees C. But, since .6 hours of the remaining diffusion time would be at 1000 degrees C, the oxides were assumed to be more than thick enough (Ref 8:213).

After etching the pattern oxides, half of wafer 5 had all the oxide etched off. This was to allow the gate predep and drive to diffuse into "virgin" silicon. After the 15 minute predep, all the wafers were four-point probed, and the average resistivity calculated. These average resistivities are shown in Table III-11.

The resistivity indicated for wafer 5** is the only good data. This resistivity results from atoms being deposited on the "virgin" silicon, producing a single doping concentration with a specific resistivity. The other resistivities,however, result from additional atoms being

deposited over a previously doped area, producing two different doping concentrations, each of which has a different resistivity. These two resistivities can be compared to two resistors in parallel, which produce an equivalent resistance that is smaller than the smallest of the two resistors.

TABLE III-11

Post Gate Predep Resistivities

Wafer 2	Wafer 3	Wafer 4	Wafer 5*
5.84	6.50	7.39	4.68

Wafer 5**	Wafer 6	Wafer 7	Wafer 8
16.16	5.77	6.71	6.29

* Note: Average of predep on previous diffusion.

** Note: One measurement on "virgin" silicon.

After the four-point probe, the gate was driven one hour instead of one and one-half hours. This was done in order to bevel and stain, and check the gate depth versus the epi. The ellipsometer photograph of the bevel and stain is shown in Figure III-6. Counting the fringing lines crossing the light area (epi) produced three lines, implying .810 microns between the gate and substrate. Counting the fringe lines crossing the first dark band produced 5.5 lines, implying the gate had diffused to 1.485 microns.

The remaining 30 minutes of drive was accomplished, and another bevel and stain performed. This time the photograph shown in Figure III-7 showed about seven lines crossing the gate, implying a total gate depth of 1.89 microns, and about 1.7 fringe lines crossing the epi, which indicated .459 microns seperating the gate and substrate and an epi depth of 2.349 microns.

Taking into consideration the amount of epi lost in the initial oxide growth, 2.349 microns reduces to an epi diffused depth of .599 microns. From these figures it appeared the boron and phosphorous diffusion coefficients were close, in that the observed diffusion depths for the epi and gate were pretty close to those calculated in Table III-1 and -3.

It was during the last 30 minutes of the gate drive that the gate oxide was grown. In order to obtain the desired 3000 angstroms in the now shorter time, the oxide growth times were changed to 4 minutes dry O_2, 23 minutes wet O_2, and 3 minutes dry O_2 (Ref 8:239-230).

Having completed the gate diffusion, the next step was to perform the source/drain diffusion.

Diffusing JFET Source/Drain

The source/drain diffusion process involved the source/drain mask photolithographic process, the etching of the source/drain pattern, and the source/drain diffusion. The actual source/drain diffusion was a n-type diffusion

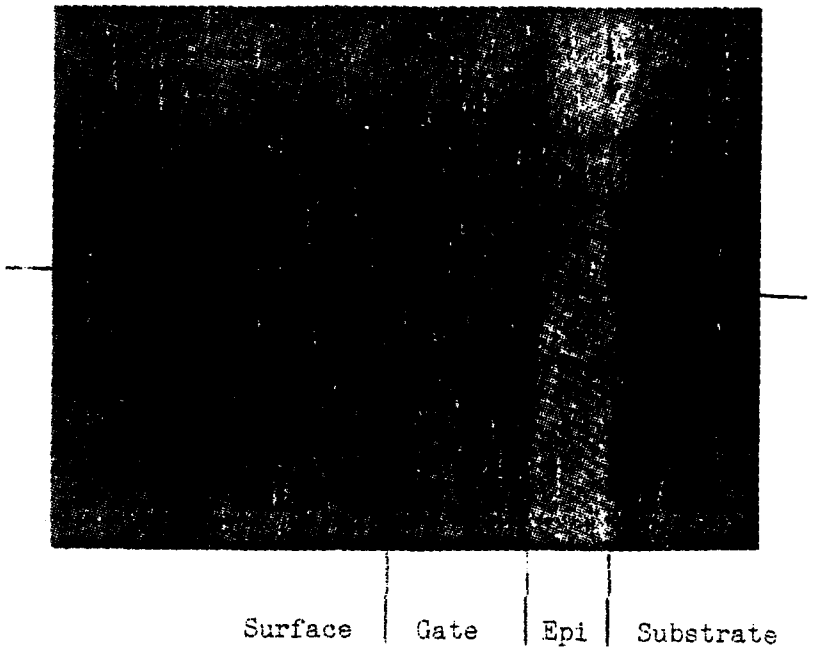

Figure III-6. Bevel and Stain of Epi-Layer and Gate After One Hour Gate Drive.

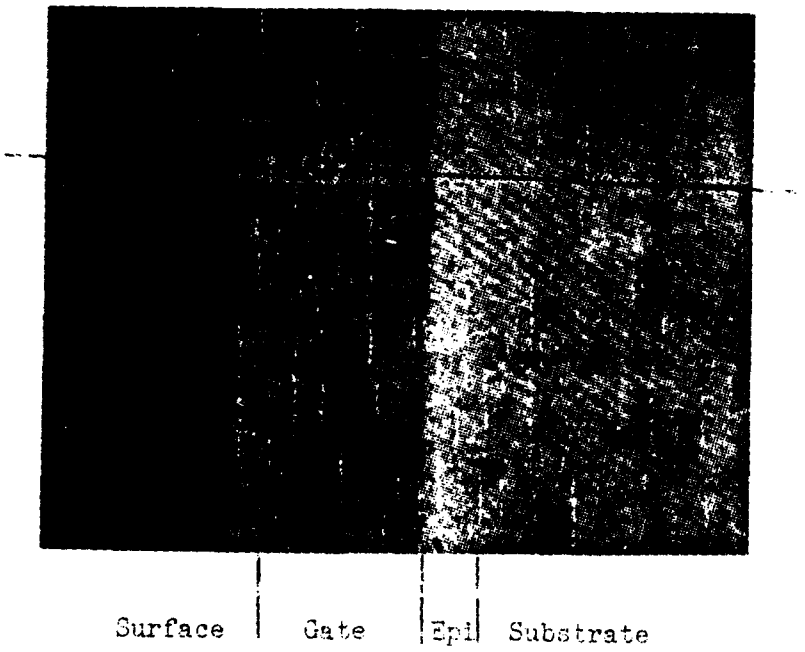

Figure III-7. Bevel and Stain of Epi-Layer and Gate After Additional Gate Drive.

into the epi.

The source/drain mask was positioned in the mask aligner, and the seven wafers surface cleaned in cleaning/etching solution CL3. The six good wafers were then processed using the photolithographic procedures outlined in Appendix C. Several iterations were done on each wafer before acceptable patterns were developed out.

Next, the oxide patterns were etched using the procedures outlined in Appendix D. After etching, the 15 minute source/drain predep was performed on the seven wafers, followed by the four-point probe. The average resistivities of the six good wafers, as well as one reading on wafer 5, are shown in Table III-12.

When the four-point probe was completed, a bevel and stain was done. The resulting photograph shown in Figure III-8, shows the source/drain diffusion versus the gate diffusion. Counting the fringe lines crossing the light area (source/drain) gave one line, which implied .25 microns.

TABLE III-12

Post Source/Drain Predep Resistivities

Wafer 2	Wafer 3	Wafer 4	Wafer 5
18.16	14.62	13.31	14.15

Wafer 6	Wafer 7	Wafer 8
13.80	14.59	17.07

It was observed that there was not a second light band (epi) between the gate and substrate. This could imply that somehow the gate drove through the epi, or that the chip just did not stain well. This photograph was taken after several attempts at staining just the source/drain.

After the bevel and stain, the source/drain was driven for 20 minutes. During this time, the passivating oxide was grown. Again, having reduced the diffusion times required the oxide growth times be changed in order to get the necessary 2000 angstroms. The new times were 4 minutes dry O_2, 12 minutes wet O_2, and 4 minutes dry O_2.

Finally, one last bevel and stain was done. The resulting photograph shown in Figure III-9, shows the final depth of the source/drain. Counting fringing lines crossing the light band gave two lines, which implied .54 microns. This source/drain depth in no way compares to that calculated in Table III-4. However, the diffusion coefficient for phosphorous at high concentrations was not corrected for the apparent error in Grove since the source/drain was the last diffusion process, and therefore allowed no chance for correction. Therefore a more conservative estimate for the diffusion coefficient was used.

It is readily apparent in this photograph that there is no second light band, and the absence of a second light band is a good indication the gate probably overran the epi.

Having completed the source/drain diffusion, the next

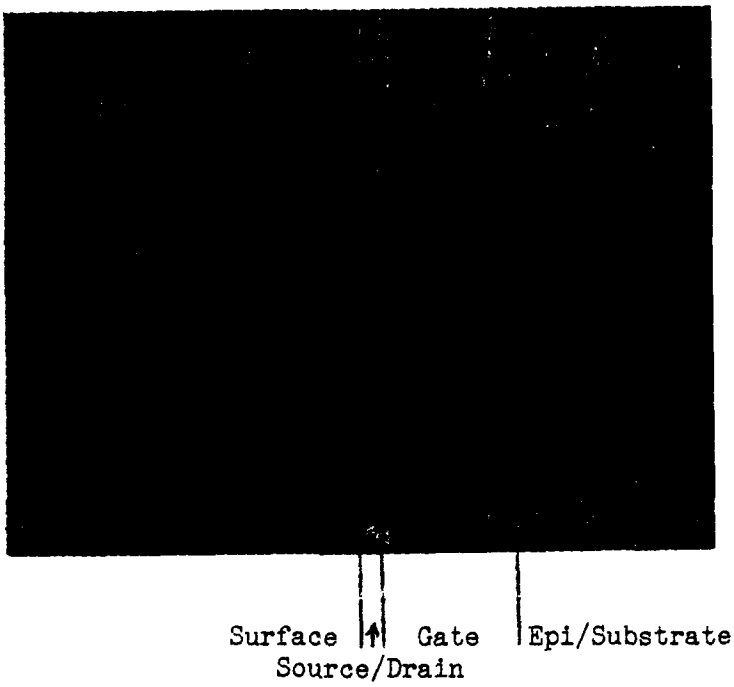

Figure III-8. Bevel and Stain of Source/Drain After Source/Drain Predep.

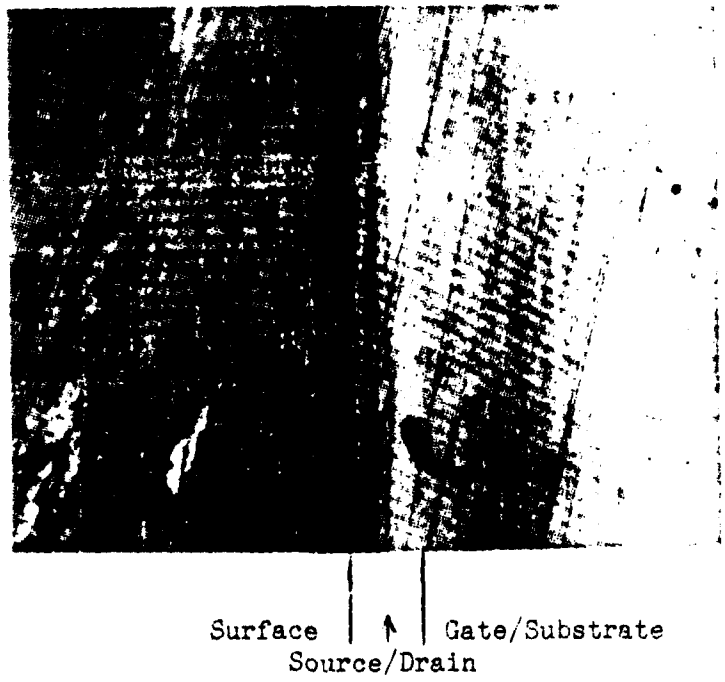

Figure III-9. Bevel and Stain of Source/Drain After Source/Drain Drive.

step was to etch the contact windows.

Etching Contact Windows

The contact windows process involved the contact window mask photolithography process, and the etching of the contact windows.

The contact window mask was positioned in the mask aligner and the six wafers surface cleaned using cleaning/etching solution CL3. The wafers were then processed using the photolithography procedures outlined in Appendix C, followed by the etching procedures outlined in Appendix D.

This concluded the contact window process, and the wafers were ready for the metallization process.

Producing Metal Pattern by Lift-off

The metallization process involved the metallization mask photolithography process and the metallization process.

The metallization mask was placed in the mask aligner, and the wafers surface cleaned in cleaning/etching solution CL3.

This procedure was somewhat different than the other masking procedures in that once the PR, in this process Shipley 1470, had been applied, exposed, and developed, there was no post baking or oxide etching. Also, the required metal was deposited on top of the PR, and then the excess metal removed through a lift-off process, leaving

just the desired metal pattern.

The mechanics of the lift-off process are to apply a layer of PR with a thickness X, and then apply the metal with a thickness Y, where Y < X. This difference in thicknesses allows acetone to attack the vertical edges of the exposed PR layer, work its way under the metal, and float the excess metal away.

During the photolithographic process, portions of the pattern were observed not to be developing out. In addition, portions of the PR were beginning to lift off. Repeated attempts were made to develop the pattern by increasing the eposure time. This increase in time resulted in better developing, but also resulted in more of the PR pattern lifting off. Two possible causes for the pattern not developing out properly may have been that the developer had weakened from standing several days, and that the PR had been affected by humidity. New develo per was mixed and a fresh bottle of PR was obtained.

New exposure and developing times had to be determined. Several iterations resulted in a 20 second exposure time and a 50 second developing time producing acceptable patterns. Using the new solutions resulted in no lifting, and only traces of PR not developing out. The wafers were then ready for the deposition of the metal layer.

The metal deposition equipment, Consolidated Vacuum Corp., vacuum deposition chamber, and a Sloan metal thickness monitor, were set up according to the

manufacturers' operating instructions (Ref 11, 12). Four of the six wafers were positioned in the chamber and a thin layer of aluminum was deposited, followed by a thin layer of silver. These two metal depositions were accomplished without breaking vacuum, thereby insuring an uncontaminated aluminum surface to which the silver could adhere.

The thickness of the metal deposited on the wafers was monitored by observing the change in frequency on the monitor. This change in frequency was due to metal being deposited on the surface of a crystal oscillator, also positioned in the chamber, resulting in a change in the ocsillator frequency. The metal thickness was then calculated from the following equation:

$$t = 2\Delta f \rho^{-1} \qquad \text{(III-2)}$$

where

t is the thickness of the deposited metal,

Δf is the change in frequency, and

ρ is the density of the metal being deposited.

During the first metallization run, the oscillator unfortunately died, and the total thickness of metal deposited could not be calculated. Both metals were deposited anyway, with hopes for the best. After the metal was completely evaporated, the current in the tungsten boat continued to flow, causing excessive heating of the PR, and

resulting in a bubbled wafer surface. However, checking the wafers under the microscope showed the metal in the patterns to be okay, so a decision to use these wafers, and to continue the metallization process was made.

The two remaining wafers were placed in the chamber, and the metallization process repeated. This time the frequency monitor functioned properly. The aluminum deposition resulted in a frequency change of 3200 Hz. Substituting this frequency and 2.7, the density of aluminum, into equation III-2 gave a thickness of 2370 angstroms. The silver deposition resulted in a frequency change of 15,500 Hz. Subtituting this frequency and 10.5, the density of silver, into equation III-2 gave a thickness of 2952 angstroms, for a total of 5322 angstroms. These two wafers did not show any indication of bubbling in the metal as the other four wafers had done. The next step was to perform the lift-off.

The first four wafers were individually placed in a beaker of acetone to lift-off the metal. After several minutes, the metal outside the patterns was observed to be lifting in places, but was not lifting satisfactorally. The wafers were placed in an ultrasonic cleaner, set at the lowest power setting, and agitated for a couple of minutes. The wafers were then removed and visually inspected under a microscope. The metal outside the pattern was seen to have lifted off, but the metal inside the pattern was not coming off. More ultrasonic cleaning was attempted, but upon

examination, parts of the metal pattern were observed to be coming off, while most of the metal inside the pattern was not. Attempts were made to lift off the metal on the other two wafers, resulting in parts of the metal patterns coming off these wafers also. Since no usable metal patterns were produced, all the metal was cleaned off the wafers, and the metallization process repeated.

The wafers were placed in cleaning/etching solution CL5 for about 30 seconds to remove all the metal, and then surface cleaned using cleaning/etching solution CL3. After the wafers were clean, the metallization mask photolithography process was reaccomplished. This time the Shipley 1350J PR was used in an attempt to obtain a thicker PR layer. The thicker PR was needed because the first metallization process probably resulted in the metal being thicker than the PR. If this were indeed the case, the acetone would not have been able to attack the PR, because the PR would have been entirely covered by the metal.

During the reaccomplishment of the photolithography process, several problems arose. The first problem was the motor of the PR spinner going out, necessitating a replacement spinner. Upon spinning the first wafer, the wafer flew off the spinner chuck, breaking into dozens of fragments. It was then determined with a stroboscope that the new spinner was actually spinning about four times faster than indicated on the meter. The speed was adjusted to show an indicated speed of '500 rpm, which provided the

required 6000 rpm.

A second problem was that the increased thickness of the new PR required a recalculation of the exposure and developing times. The new PR was much more difficult to process, however, several photolithography iterations resulted in 30 seconds exposure time and 60 seconds developing time producing acceptable patterns. As was the case in earlier attempts, traces of PR were observed in the patterns after developing. The wafers were again ready for applying the metal.

At this point only four wafers were left to apply metal to (another one broke in processing). The four wafers were placed in the vacuum chamber, and the aluminum and silver deposited. This time the frequency changes were 1800 Hz and 10,500 Hz for aluminum and silver respectively. Substituting these frequencies into equation III-2 produced 1333 angstroms of aluminum and 2000 angstroms of silver, yielding a total of 3333 angstroms. The wafers were again ready to attempt lift-off.

This attempt at lift-off did not produce much better results than the first attempt. Metal still would not lift out of the patterns, and ultrsonic cleaning resulted in some bonding pads, and pieces of pattern coming off, as well as the unwanted metal. Several patterns were finally produced that would allow probing of the transistors with a transistor curve tracer and probe station to determine the transistor characteristics. That is providing, of course,

the gate had not been driven through the epi, and a JFET transistor had indeed been produced.

It should be pointed out that subsequent to this thesis effort, the metal lift off process was perfected. The key to success lies in stopping the current flow through the tungsten evaporation boat as soon as, or just before, all the metal has evaporated. The thickness monitor used in the metalization process does not give a suitable indication as to when the metal being vaporized is about to be used up. A much more accurate method, for monitoring the point at which the metal is depleted, is to use a deposition rate meter. While metal is available in the tungsten boat, and being vaporized, the rate meter needle will indicate some upscale reading that is proportional to the amount of current flowing through the boat. Just before the metal is completly vaporized, the needle will swing slightly farther upscale. At the time the metal is completely vaporized, the rate meter needle will go to zero.

While there was a deposition rate meter available, unfortunately it was not used for the wafers in this thesis.

CHAPTER IV

TEST AND ANALYSIS OF JFET ARRAY

Testing the JFET Array

Having produced some probeable "JFETs" in the metal pattern, a wafer was placed in the probe station. Four probes were used to contact the JFET's source, gate, and drain, and the substrate through the isolation. The probes were then connected to a transistor curve tracer, which was set up to display JFET transistor characteristics. No typical transistor curves were noted.

Table IV-1 below, shows the electrical characteristics one should obtain, as well as the characteristics that were actually obtained.

TABLE IV-1

JFET Characteristics

	Forward Biased		Reversed Biased	
	Should Obtain	Actually Obtained	Should Obtain	Actually Obtained
Source-Gate	diode	diode	open	open
Source-Drain	resistor	open	resistor	open
Drain-Gate	diode	diode	open	open
Substrate-Source	diode	diode	open	open
Substrate-Gate	open	resistor	open	resistor
Substrate-Drain	diode	diode	open	open

An isometric, quarter cut-away of the general JFET configuration is shown in Figure IV-1 to aid in visualizing the points being checked.

It seems apparent from the substrate to gate reading that the gate went through the epi and contacted the substrate, resulting in a p-type channel between the substrate and gate. Another indication that the gate went through the epi is the source to drain reading. If the gate had not gone through the epi, there would have been a resistive path, through the epi, between the source and drain. If the gate did go through the epi, the resistive path would have been replaced by two back to back p-n junctions resulting in an open, as was the case.

The remaining point to point checks showed the rest of the characteristics to be as they should. An attempt was then made to determine why the gate would have gone through the epi.

Analyzing the JFET Array

In trying to determine what had happened to the gate, the calculations of Tables III-6 and -8 were reexamined. From the depths indicated in the tables versus the depths measured in the photographs, one of three things possibly happened: (1) Either the boron gate diffused faster than calculated, indicating the diffusion coefficient was to small; (2) the phosphorous epi diffused slower than

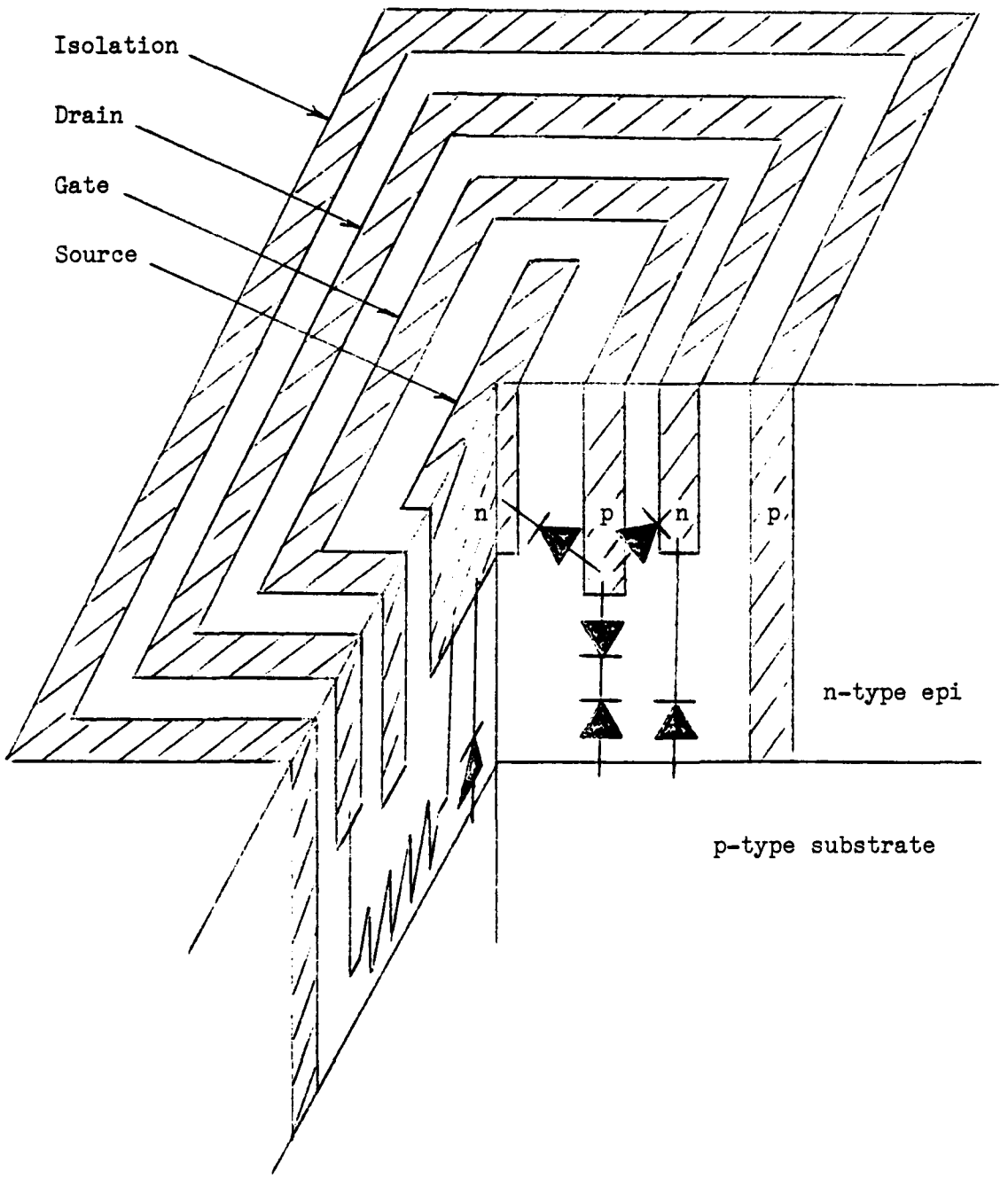

Figure IV-1. Isometric, quarter cut-away of JFET.

calculated, indicating the diffusion coefficient was too big; or (3) both. An initial test was performed to determine if the boron diffusion coefficient was correct

Equation II-5 was solved for x_j, given that the gate drive was for only one hour. The result was compared to the measured depth of the gate, according to Figure III-6. The calculated depth of 1.5125 microns when compared to the measured depth of 1.485 microns resulted in a difference of .0275 microns, or 275 angstroms. This difference amounts to one-tenth of a fringe line, which cannot be accurately measured from the photograph. It would appear the diffusion coefficient for boron was almost exact, at least at 1050 degrees C.

Assuming an initial oxide of 5000 angstroms, of which 50% came from the epi, may have been the culprit since the actual oxide ranged from 4545 to 4385. Taking the 4345 as the worst case, and that 45% came from the epi results in 1973 angstroms of epi being consumed, leaving 1.8027 microns instead of 1.755 microns. Using this new value, and the measured epi depth of 2.295 microns from Figure III-6, results in the epi actually diffusing only .4923 microns instead of the calculated .5967 microns from Table III-6. Using .4923 microns, equation II-2 was recomputed, giving a diffusion coefficient for phosphorous of 1.7491×10^{-14} $cm^2\text{-}sec^{-1}$. This value is approximately 71% of what was used in the computations for the epi diffusion at 1050 degrees C in Table III-6.

With the epi measured at 2.295 microns and the gate measured at 1.5125 microns, this left .7825 microns between the gate and the epi after one hour of base drive in. The calculations of Tables III-6 and -8 indicated a distance of .8199 microns, which is a difference of only 374 angstroms. Therefore, it does not appear that a significant error resulted from miscalculating because of a wrong assumption concerning the oxide.

The other possibility seems to be that either one or both of the diffusion coefficients for boron and phosphorous at 1000 degress C are wrong. Unfortunately these diffusion coefficients can not be checked as photographs by which to measure the actual depth could not be made.

One additional possibility was considered. Checking in Grove, it was found that the epi space charged depletion region for this particular device was approximately 0.5 micron with no bias applied. In order for the JFET to work properly, the gate channel thickness needed to be around one micron. This increased channel thickness would have resulted in an effective channel thickness of about one-half micron (Ref 7:163). This seems at this point to be the most probable cause since there is no indication from the calculations that an error was made.

CHAPTER V

DESIGN SUMMARY AND TEST OF MULTIPLEXERS

Summary of Multiplexer Design I

The first multiplexer design (Figure V-1) consists of four major building blocks; a count selectable counter, a sixteen output row multiplexer, a decoder, and a sixteen by sixteen multielectrode array. Inputs to the system include; system clock (NCLK), sync in (SYI), and count select (CS) 0, 1, and 2. Outputs from the system are sync out (SYO), and sixteen column out (CO) signals.

This multiplexer design has several additional input/output features intended for testing purposes. These features include: $\emptyset_1$ and $\emptyset_2$ pads, four tri-state (TS) buffer pads and associated control (CON) pad, and sixteen multiplexer select out (SO) pads. These features are explained in "Testing".

The count selectable counter either counts sequentially through a defined count sequence, or presets to a single count state as defined by the counter's inputs. The counter generates four next state (NS) outputs that feed back to the counter, and feed forward to the row multiplexer and the decoder.

The multiplexer inputs the four NS signals and selects the corresponding one of sixteen SO outputs. Whenever an SO line is selected, it goes high, while the other fifteen SO lines are low. The SO lines each control the output of an

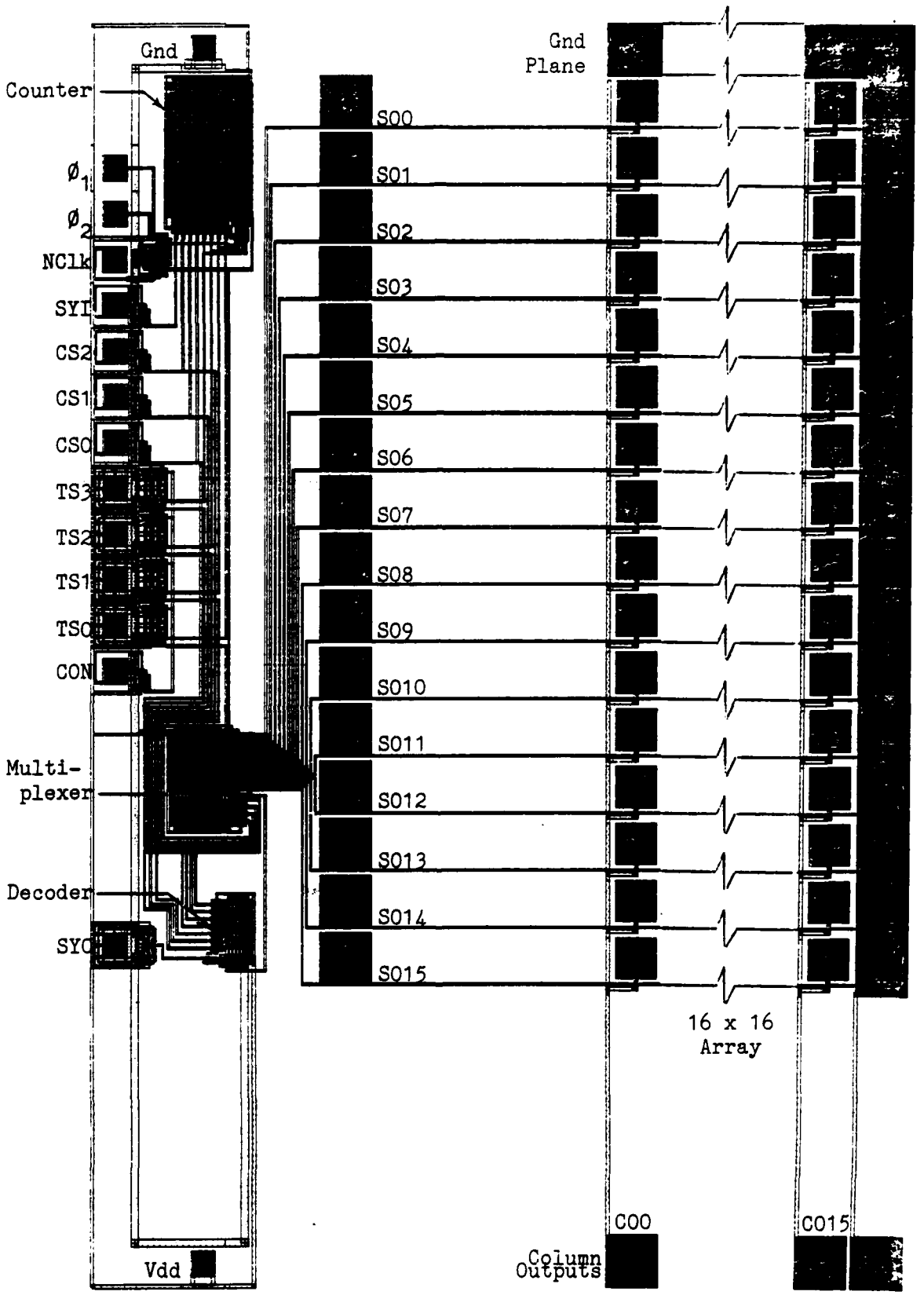

Figure V-1. Schematic of Multiplexer Design I (Scale: 325 micron per inch).

entire row of electrodes in the array.

The decoder inputs the four NS signals, as well as the three CS signals. Whenever the count state of the NS signals corresponds to the maximum count of the count sequence defined by the CS signals, the decoder output, SYO, goes high.

Each row of the multielectrode array is connected to one of the multiplexer SO lines. As each SO line is selected, the corresponding array row is enabled, outputting in parallel the signals sensed by each of the sixteen electrodes.

One important feature of the this multiplexer design that is not included in Multiplexer Design II, is the provision for scribing and breaking the chip between the SO pads and the array. This provision allows the use of the NMOS multiplexer circuit with various other sizes and types of arrays. Specifically, the four by four JFET array. Used in this manner, the SO pads serve as the wire bonding pads between the multiplexer and the array.

Summary of Multiplexer Design II

The second multiplexer design (Figure V-2) consists of six major building blocks; a count selectable counter, a sixteen output row multiplexer, an expanded decoder, a four-bit counter, a sixteen output column multiplexer, and a sixteen by sixteen electrode array. Inputs to the system include; SYI, three CS signals, and NCLK. Outputs from the

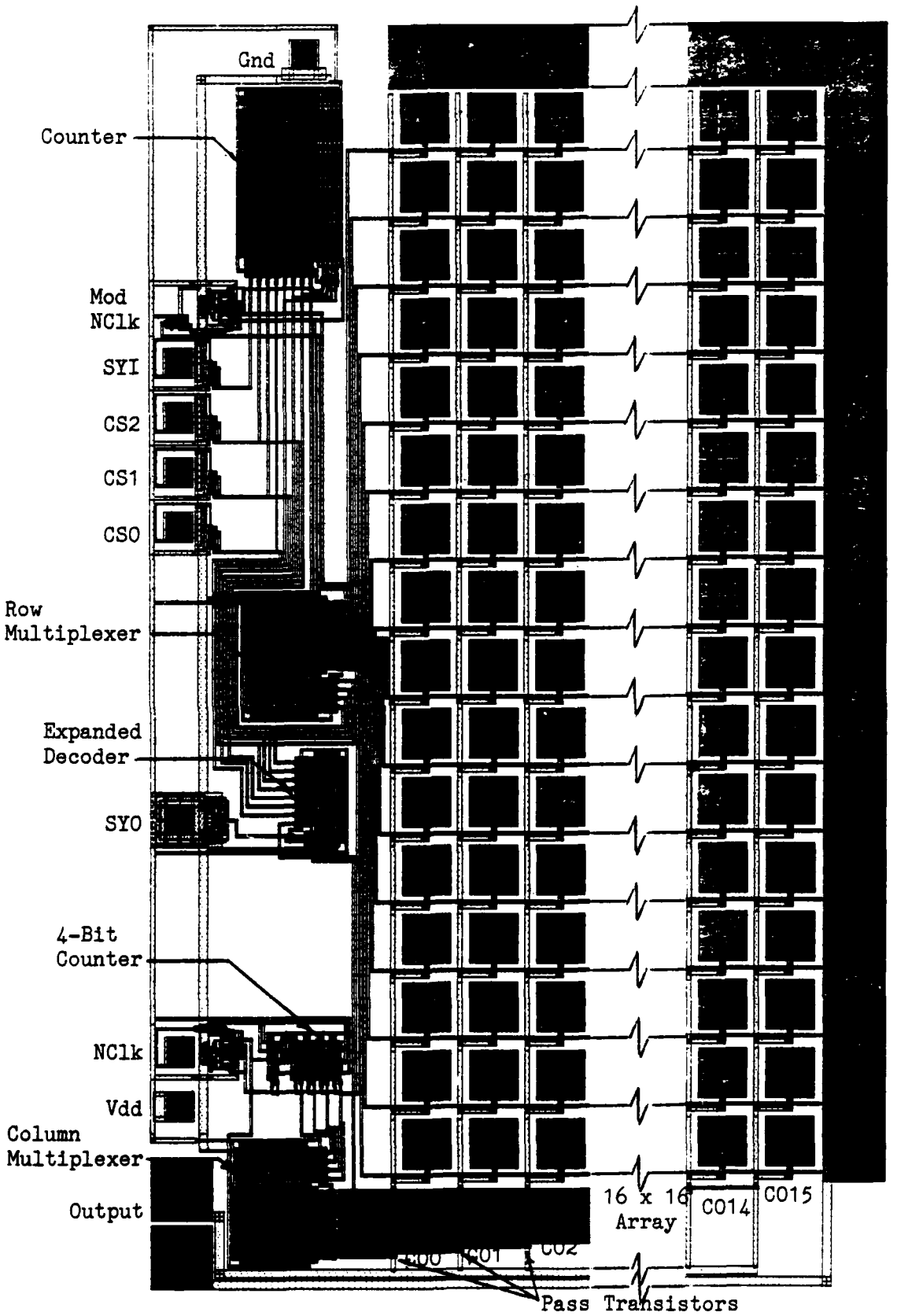

Figure V-2. Schematic of Multiplexer Design II (Scale: 272 micron per inch).

system are; SYO, and OUTPUT.

This multiplexer design does not have any of the test features included in the first multiplexer design. It was felt that if the first design worked, this design would also.

In this design, the count selectable counter and row multiplexer function exactly the same as in the first design. The expanded decoder also functions the same, except it includes an additional input; column out (CO) 15 from the column multiplexer. The expanded decoder will not output SYO, for any given input, until CO15 is high.

The four-bit counter inputs NCLK and generates four output bits, which go to the column multiplexer, and serve the same purpose as the NS signals to the row multiplexer. In addition, the most significant bit (Bit 4) of the four-bit counter goes to the modified clock pad (Mod NCLK), generating two phases that clock sixteen times slower than the system input clock.

The column multiplexer inputs the four bits of the four-bit counter, and selects the corresponding one of sixteen CO outputs. Whenever a CO line is selected, it goes high, while the other fifteen CO lines are low. The CO lines each control the output of a single column of electrodes in the array.

Each output column of the electrode array is enabled as the column multiplexer sequences through the CO selection. It turns out that because of the different clocking speeds,

the CO lines are clocked sixteen times faster than the SO lines. This results in a conversion from a parallel output to a serial string output.

The above has been a brief summary of the two different multiplexer designs. A more detailed explanation of the individual building blocks is contained in Appendix G. For a detailed explanation of the overall design, see "Report on Brain Chip Array with Count Selectable Multiplexer" (Ref 21).

Testing Multiplexer Design I

The following is a summary of the testing performed on Multiplexer Design I. For the complete test procedures and results see "Final Report on Test Results of Multiplexed Brain Chip Array (Ref 22).

Initially, the chip was visually checked under a microscope for fabrication defects and/or design errors. No errors or defects were noted. Next, power and ground were applied to the chip in order to measure the operating current under static conditions. This current was measured at 18 milliamps.

After the initial tests, the chip was inserted in the test circuit with power, ground, and all input signals applied. With an oscilloscope, the various signals were observed to verify whether or not each of the building blocks was functioning properly.

First, the clock phases at the ϕ_1 and ϕ_2 pads were

observed and compared to the clock input to NCLK to check for proper operation of NCLK, and proper phasing of its ϕ_1 and ϕ_2 outputs. NCLK was noted as operating properly. If NCLK had not been operating properly, two phases could have been supplied externally through the ϕ_1 and ϕ_2 pads.

Second, the count selectable counter was fully checked out by manually switching the various input combinations of the SYI and CS signals, and observing the NS outputs at the TS pads. In all instances, the counter was noted as operating properly. If the counter had not operated properly, psuedo NS signals could have been input externally through the TS pads, thereby allowing proper functional testing of the row multiplexer and the decoder.

Third, having verified the counter operation, the SYO signal was observed to insure proper decoder operation while again switching the SYI and CS inputs. In all instances, the decoder was noted as operating properly.

Fourth, the row multiplexer SO lines were observed at the SO pads for proper sequencing while all SYI and CS switch combinations were again tried. The multiplexer functioned properly as far as the selection sequencing went, however, a symptom of a major problem with the multiplexer was noted. While the selected SO line would go high as it should have, the other fifteen SO lines were observed to have a positive 1.2 volt dc offset. This offset resulted in the entire array being continually enabled, making it unusable. Without knowing what the immediate problem was

with the multiplexer, the electrode array was tested.

Finally, by bonding wires to the electrodes and injecting a sinusoidal signal onto the electrode, and observing the CO pads, the array functioned properly under the circumstances. Because of the offset, any signal injected onto the electrode, with an amplitude less than 1.2 volts, appeared continually at the output. However, if the amplitude of the injected signal was greater than 1.2 volts, any portion of the signal outside the selected SO pulse width was clipped. This clipping resulted in that portion of the injected signal within the bounds of the SO pulse appearing at the output, while the portion of the signal outside the pulse width appeared at the output with a maximum amplitude of 1.2 volts. This infered that if the multiplexer SO lines went to 0 volts, as they should when not selected, only that portion of the injected signal falling within the SO pulse width would appear at the output.

Having verified the operation of the entire chip, further testing was performed in an attempt to determine the cause of the multiplexer problem. The problem was possibly a bad ground connection between the multiplexer and the ground line. At this point another visual test was performed under the microscope with no apparent defect observed. Next, an attempt was made to probe the multiplexer ground wire, but since the chip was covered with a passivating glass layer, and at best the wire was only

eight microns wide and only six microns away from other wires, this attempt proved to be futile.

No definite solution to the problem was found, although it is believed that a design error is the cause of the problem. The ground wire was made of a diffused region instead of metal. Typically, diffusion has a resistance of approximately 10 ohms per square, while metal has a resistance of approximately 0.03 ohms per square. The diffusion was eight microns wide and 144 microns long, resulting in 18 squares or a resistance of approximately 180 ohms. A metal wire on the other hand would have an approximate resistance of .54 ohms (Ref 23:51).

Having no better explanation as to the problem, the ground connection was redesigned. The multiplexer ground connection in both multiplexer designs was changed to metal, and the two new designs resubmitted for fabrication. Future testing will verify whether or not the ground connection was indeed the problem.

CHAPTER VI

CONCLUSIONS AND RECOMMENDATIONS

Conclusions

For all practical purposes, only one conclusion can be drawn from this thesis: According to the calculations and photographs of Chapter III, the JFETs should have worked.

This thesis project was an attempt to produce a set of JFET Arrays on three inch wafers, using standard integrated circuit fabrication techniques. While the techniques may be standard, in the lab environment it was extremely difficult to maintain repeatability.

The biggest problem in the lab was dust. Many times dust on the wafers, or the mask, caused a repeat of the photolithographic process. Another problem was not having the proper size beakers for cleaning/etching the wafers. If the beakers had been available, some of the cleaning/etching processes could have been accomplished simultaineously on all the wafers instead of one at a time. Finally, one additional problem was not having the proper wafer boats with which to perform the boron and phosphorous drives.

One mistake made early in the project was not using the test wafers to determine the diffusion coefficients before starting the actual fabrication. If the diffusion coefficients had been determined early, there would have been enough time in the diffusion processes to make better corrections if needed. The biggest mistake, however, was

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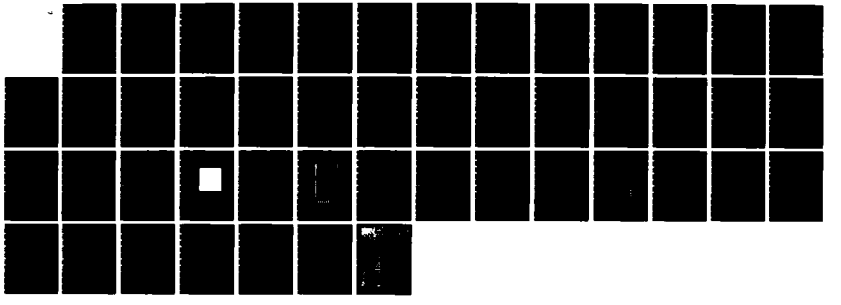

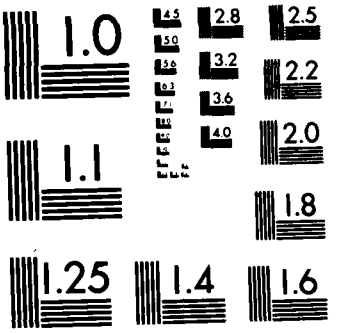

not considering the thickness of the space charge depletion region, and allowing for it in the gate diffusion calculations.

Finally, the NMOS array looks promising in regard to two important factors. First, all the pass transistors of the array have essentially the same electrical characterisitcs, whereas the JFET array transistors have widely varying reverse leakage currents, resulting in a dc offset on the output signals. Second, the pass transistors of the NMOS array can be made much smaller than the JFETs, thereby making much more of the chip available for other circuitry.

Recommendations

This thesis project was at least three months late getting started due to the absence of functioning equipment. Therefore, the first recommendation would be - make sure all the equipment is available and operational, long before the tenative start date, including the little pieces of equipment, like proper size beakers, adequate wafer holders, and proper diffusion boats. A lot of the little pieces had to be scrounged, and for the rest - had to make do the best way possible.

The second recommendation is to use some other reference besides Grove for obtaining the initial diffusion coefficients. As can be seen from Chapters II and III, the diffusion coefficient for boron was about 50% of what it

should have been to start with, and the diffusion coefficient for phosphorous was about 150% of what it should have been. By the time it was realized just how bad Grove's diffusion coefficients were, it was almost too late to recover.

The third recommendation is to have the student get out of the integrated circuit fabrication business, and have the fabrication done by a commercial company. The commercial fabrication facilities are prepared to perform this kind of semiconductor processing.

The fourth recommendation is to pursue the NMOS multiplexer array, and either drop the JFET array, or put considerably less emphasis on it if possible. The savings in real estate alone will allow more functions to be implemented with the NMOS design.

The fifth and final recommendation is to investigate the feasibility of incorporating differential amplifiers into the NMOS array. At the present, roughly 25,600 square microns under each array electrode are being wasted. If an amplifier could be situated beneath each electrode, the requirement for a high gain external amplifier should be eliminated. In addition, by amplifying the signal right at the pad, before sending it out the column output, the signal to noise ratio should be increased considerably. Also, by placing a differential amplifier between adjacent electrodes and comparing signals, (i.e signals 1 and 2, 2 and 3, etc.), any dc offsets would be eliminated.

Should someone is the future undertake a similiar project, here are some recommended do's and don'ts.

DO - Make several test oxidations and diffusions, to include both boron and phosphorous. Work out the bugs, and determine the actual diffusion coefficients before fabrication. There should be test runs at all temperatures that will be used in the final project.

DO - Get all the necessary beakers, wafer holders, diffusion boats, and the like, for three inch wafer processing; it will eliminate some of the frustrations and help make the effort run a little smoother.

DO - Get the photolithography room cleaned out and cleaned up. Eliminate as much clutter as possible, and the result should be less dust.

DO - Four-point probe the test wafers thoroughly, maybe in a dozen or more places, in order to get a true profile of how the dopant is being deposited during predep. Once the test runs are done, forget about probing the actual wafers since the characteristics are already known.

DO - Perform ellipsometer checks over different areas of the test wafers, not just in the middle, to get a true picture on how uniform the oxide thickness is on a particular wafer, and between wafers.

DO - Perform the diffusion predep immediately after the etching is complete rather than letting the wafers stand overnight or a day or more. In addition, perform the diffusion drive immediately after the predep.

DON'T - Make assumptions in any calculations. Be as precise as possible, but not to ten decimal places.

DON'T - Four-point probe the actual circuit wafers. The characteristics of the furnace should already be known, and besides, in all probability the wafer will be covered with oxide and cannot be probed anyway.

DON'T - Surface clean to much. If the amount of dust is cut down, and proper handling techniques are employed, the wafers won't need surface cleaning anyway.

DON'T - Make the same mistakes others have made. Check out the best way to perform a particular process, and avoid the pitfalls of having to reinvent the wheel.

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APPENDIX A

DUPLICATING A REVERSED IMAGE MASK SET

Duplication of the mask set was performed at the Avionics Laboratory, AADE-3, Wright-Patterson Air Force Base, Ohio. The new reversed mask set was required because previously (-) photoresist (PR) was used, and (+) PR was used in this thesis. The new mask set has a clear pattern and a dark field. The procedures for making a reversed mask are as follows.

Mixing the Developer

Following Kodak's instructions, mix one package of Part A, Kodak Developer D-8, with one package Part B, Sodium Hydroxide (NaOH).

Setting Up the Contact Printer

Using an Ultra Tech Corporation Contact Printer, set the controls as follows.

a. Plate Separation Time - 1.5 seconds.

b. Vacuum Pump Down Time - 2 seconds.

c. N_2 Purge Time - .25 seconds.

d. Emulsion Intensity - 5.

e. Photoresist Intensity - 7.

f. Lamp Servo Mode Switch - Normal.

Making the Mask Print

To make a contact print of an existing mask, perform the following steps.

a. Turn on the Main Power to the contact printer.

b. Position the mask to be copied in the mask holder.

c. Turn on the Master Vacuum (20 psi) to hold the mask in place.

d. Position the plate, Kodak 4"x4"x.060" KP65774 High Resolution Plate, in the plate holder.

e. Close the door of the contact printer and observe the Cycle On indicator is lighted, and the vacuum gauges read approximately 25 psi.

f. When the Cycle On indicator goes out, open the contact printer door, and remove and develop the plate.

g. Repeat the above steps for each additional plate to be copied.

Developing the Mask Print

To develop the plate, perform the following steps.

a. Place the plate in the developer for 2 minutes.

b. Remove the plate from the developer and place in the stop bath for 30 seconds.

c. Remove the plate from the stop bath and place in the fixer for 2 minutes.

d. Remove the plate from the fixer and rinse in de-ionized water (DIW) for 30 seconds.

e. Remove the plate from the DIW and place in a 50/50

solution of DIW and methyl alcohol for 2 minutes.

f. Remove the plate from the 50/50 mixture and place in 100% methyl alcohol for 2 minutes.

g. Remove the plate from the methyl alcohol and blow dry the plate with dry N_2.

h. Inspect the plate under a microscope for definition of pattern and any apparent defects.

i. Scrub the plate with methyl alcohol and a cellular foam swab to remove any residue, rinse the plate in DIW, and blow dry the plate with dry N_2.

j. Repeat the above steps for each additional plate to be developed.

This concludes the procedures for making a reversed image contact mask print.

APPENDIX B

CLEANING/ETCHING SOLUTIONS AND USES

The following is a list of the standard cleaning and etching processes used during this fabrication. Ratios for mixing chemicals are indicated, rather than specific amounts, as the amount of a solution required depends on the type and size of beaker, and type and size of wafer holder.

CL1: This cleaning process uses sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2), di-ionized water (DIW), hydrofluoric acid (HF), and nitrogen (N_2).

3:2, H_2SO_4:H_2O_2	15 minutes
DIW rinse	5 minutes above 10 megohms
10:1, DIW:HF	15 seconds
DIW rinse	5 minutes above 10 megohms
N_2 blow dry	as required

The first solution is self-heating, which generates a bubbling action when mixed, and should be used while bubbles are present. The solution is used primarily on new wafers to remove any organic materials that may be present. The second solution is used to remove any inorganic materials, primarily silicon dioxide, from the new wafers.

CL2: This cleaning process uses nitric acid (HNO_3), DIW,

HF, and N_2.

HNO_3 (boiling)	30 minutes
DIW rinse	5 minutes above 10 megohms
10:1, DIW:HF	10 seconds
DIW rinse	5 minutes above 10 megohms
N_2 blow dry	as required

The boiling nitric is used to remove the borosilicate glass layer formed on the wafer surface during the boron predeposition. The second solution removes any oxide from the wafer surface that may have grown during the nitric bath.

CL3: This cleaning process uses DIW, HF, and N_2.

10:1 DIW:HF	10 seconds
DIW rinse	5 minutes above 10 megohms
N_2 blow dry	as required

This solution is used to clean the wafer surface of any contaminants and oxide that may have accumulated on the wafer surface during, or between, processes.

CL4: This cleaning process uses ammonium fluoride (NH_4F), HF, DIW, and N_2.

6:1, NH_4F:HF	as required
DIW rinse	5 minutes above 10 megohms
N_2 blow dry	as required

This solution is used to remove the oxide in the mask pattern. After mixing the solution, it should stand for two hours to stabilize prior to use. Normally it etches silicon dioxide at a rate of approximately 1000 angstroms per minute. The solution is a buffered solution, and is therefore more gentle on the photoresist than CL3.

CL5: This cleaning process uses DIW, phosphoric acid (H_3PO_4), HNO_3, and glacial acidic acid (HAc).

19:17:1:1, DIW:H_3PO_4:HNO_3:HAc	as required
DIW rinse	5 minutes above 10 megohms

This solution is used to remove all the metal from the wafer in the event the metallization process must be reaccomplished. To use, place the solution on a hot plate and heat to 60-65 degrees C.

APPENDIX

DETERMINING PHOTOLITHOGRAPHY PROCEDURES

Many interrelated factors determine whether a photolithographic pattern developes, and subsequently etches, with satisfactory results. Among these factors are: How well the photoresist (PR) adheres to the wafer, type of PR used, the thickness of the PR layer, how the PR is applied, how long the PR is exposed, how long the PR is developed, and how easily the PR is removed after etching. Each of these factors was investigated and resolved as explained below.

First, how well the PR adheres to the wafer depends on how dry initially the wafers are, how resistant the PR is to lifting off, whether an adhesion promoter is used, and how long the PR is baked. To insure the wafers are completely dry, they are baked out in an oven at 220 degrees C for at least one hour. Then, as a precaution (Ref 8:242), an adhesion promoter is applied to the wafers: Hexamethyldisilasane (HMDS) Electronic Grade, Organic Chemicals Division, SCM Corp. Next, the PR is applied to the wafers using a spinner, the wafers are pre-baked at 70 degrees C for 10 minutes to dry the volatiles in the PR, the wafers are exposed 12 to 20 seconds at 275 watts, and then the wafers are post baked at 100 degrees for 30 minutes to dry out the PR and toughen it prior to the etching process. After etching, the PR is removed with acetone.

After the first attempts with the PR, it was discovered that it would not come off in the acetone. It was later learned that the degree of toughness is a time-temperature product (Ref 24), and that either baking to long (total) or at too high a temperature made the PR too tough to remove. Therefore, combinations of lower temperatures and shorter times were tried until the PR would come off easily in the acetone, yet was tough enough to withstand the etching solution.

Second, the thickness of the PR is determined by its viscosity, and the rate of spin and length of spin time. Two different positive PRs were tested: Microposit™ Photoresist 1350J and Microposit™ Photoresist 1470, Shipley Co., Inc. The 1350J has the higher viscosity, resulting in a thicker layer, and since resistance to liftoff is also a function of thickness, the 1350J was tried first. It was found that, because of such small pattern geometries, the thicker PR pattern would not develop properly unless exposure and developing times were increased to well over one minute each. Even at best, though, the smaller pattern geometries would only develop to about one-half the required size, proving to be totally unacceptable. The 1470 was then tried with significantly better results.

With both PRs, different spin rate/time combinations were tried in order to get a uniform thickness of PR across the wafer surface. If the spin rate is too high and/or the time is too long, most of the PR is slung off the wafer,

resulting in too thin a layer. On the other hand, if the spin rate is too slow and/or the time is too short, the PR collects at the edge of the wafer, sets up, and results in a non-uniform, dished, layer. This dishing effect prevents the wafer from completely contacting the mask during the exposure, resulting in a distorted pattern. The uniformity of the PR layer was checked by bringing the wafer into contact with the mask and observing that light diffraction lines (rainbow pattern) covered the entire wafer surface. The spin rate and time were adjusted until these diffraction line patterns were observed.

Finally, different combinations of exposure and developing times were tried, to produce the best patterns. Since the 1470 PR layer was thinner, it did not require as long an exposure or developing time. Long exposure times result in shorter developing times, but may over expose the PR, causing wider and less distinct (fuzzy) pattern lines due to light diffraction. Short exposure times require longer developing times, and can result in over developing, which causes loosening of the PR with subsequent lifting. Initially, developing was attempted by puddling the developer on the wafer, letting it stand, and then spinning the wafer to remove the developer. However, in too many instances, portions of the PR pattern would lift off, and the entire process would have to be reaccomplished. It was found that simply tilting the wafer and allowing the developer to run off, proved satisfactory. After many

iterations of applying, exposing, developing, and removing photoresist, the following baseline procedures were defined.

a. Bake wafers at 220 degrees C for one to two hours to remove all moisture.

b. Set the speed control on the Headway Research Inc., Model EC101, spinner to 6000 rpm.

c. Set the time control to 15 seconds.

d. Place wafer on spinner chuck, depress start pedal, and blow off any surface dust with dry nitrogen.

e. When spinner stops, apply 4-5 drops adhesion promoter, Organic Chemicals Division, SCM Corp., Hexamethyldisilazane (HMDS) Electronic Grade, to the center of the wafer and spin.

f. When the spinner stops, apply 8-10 drops photoresist, Shipley Co., Inc., Microposit™ 351 Photoresist (positive) 1470, to the center of the wafer and spin.

g. When the spinner stops, place wafer in oven and pre-bake at 70 degrees C for 10 minutes to remove volitales from photoresist.

h. Remove wafer from oven and allow to cool.

i. Place wafer on mask aligner chuck, align pattern and expose wafer for 12 seconds.

j. Remove wafer from aligner, place on spinner chuck, flood wafer with a 4:1 mixture of DIW:developer, Shipley Co., Inc., Microposit™ 351 Developer, and allow to develop for 30 seconds.

k. Tip the wafer to remove developer, rinse off remaining developer with DIW, and VERY GENTLY blow dry with dry nitrogen.

l. Examine the pattern under a microscope. If the pattern is not sufficiently developed, repeat step j for 15 seconds and recheck pattern. If any photoresist lifts off (where it is not supposed to), remove the entire layer of photoresist with acetone. Rinse off the acetone with methyl alcohol, and rinse in running DIW. Repeat all above steps with step a being only 1 hour.

m. When all wafers are developed, post-bake the wafers in an oven at 100 degrees for 30 minutes to dry the photoresist and toughen the photoresist surface.

n. Etch the oxide pattern (see Appendix D).

APPENDIX D

DETERMINING OXIDE ETCHING PROCEDURES

Several test wafers were processed through the photolithographic process to obtain a pattern (see Appendix C). These wafers were then etched to check the rate of the etching solution, and the toughness of the photoresist (PR). Initially, cleaning/etching solution CL3 (see Appendix B) was used to etch the pattern oxide. However, this presented two problems: First, the etch rate was not predictable with any accuracy. Second, the solution seemed to be too harsh for the PR, and lifting of the PR occured before the pattern was completely etched.

Next, a buffered solution, cleaning/etching solution CL4, was tried. When first mixed and used, the etch rate was considerably different for successive wafers. The first wafer etched quickly, while the last wafer etched much more slowly. After several attempts, it was found that by allowing the solution to set and stablize two hours after mixing, the etch rate was more uniform between wafers; approximately 1000 angstroms per minute. However, the solution appears to lose its effectiveness with time (several hours), and a new solution has to be mixed on at least a daily basis.

The etch rate was checked by first determining the thickness of the oxide to be etched. This was done by knowing approximately how much oxide was grown, and then

checking the oxide color under a microscope. The observed color was then cross-checked against an oxide color chart. This helped establish the actual thickness of the initial oxide. A wafer was then immersed in the etch solution for one minute, removed, dried, and visually checked under a microscope for color change. Each color change corresponded to a specific oxide thickness. By repeating this process several times, the etch rate of the solution was calculated.

It was also determined that the PR could be subjected to total etch times in excess of five minutes without any appreciable lifting. It was observed though that after the five minutes, there was slight lifting of the PR around the edges. This was not a problem, in that most of the oxide was etched out before the five minutes elapsed.

After etching several wafers, the following procedures were found to give satisfactory results.

a. Mix sufficient quantity of cleaning/etching solution CL4 to cover wafer (amount will depend on size of container and wafer holder).

b. Let the solution stand for 2 hours.

c. Place the wafer to be etched in the solution and allow to etch for the desired time. For example, 2000 angstroms of oxide at an etch rate of 1000 angstroms per minute implies an etch time of two minutes.

d. Remove the wafer from the etch, rinse throughly in running DIW (about 10 seconds), gently blow dry with dry

nitrogen, and examine the pattern under a microscope.

e. If the pattern is not clear of all oxide, repeat etchings of 15 second increments until all pattern oxide is removed.

f. When all wafers have been etched, remove the PR with acetone, rinse the wafers with methyl alcohol, and rinse the wafers in running DIW for about 10 seconds.

g. Clean the wafers with cleaning/etching solution CL3 and proceed with the diffusion process, if required.

APPENDIX E

PREPARING THE DIFFUSION FURNACE

This thesis project involved the use of a new Thermco Products Co., furnace for three inch wafers, and therefore required that each of three tubes, oxide, p-type, and n-type, be profiled to establish a flat temperature zone. It was decided the temperatures would be: 1050 degrees C for the initial oxidation, 1050 degrees C for the boron (p-type) diffusions, and 1000 degrees C for the phosphorous (n-type) diffusions.

Each tube has three resistive heating elements, and each element has a dedicated temperature controller and associated thermocouple. The thermocouples are not that accurate, so external thermocouples and a digital meter were used. Each controller controls the temperature of one of three zones: Source zone, the zone farthest from the open end of the tube; center zone; and load zone, the zone closest to the open end of the tube.

The external thermocouple, when placed inside the tube, was only long enough to extend five and one-half inches past center. Therefore, it was decided that only an eleven inch flat zone (five and one-half inches left and right of center) would be used. The thermocouple was positioned in the tube so the end of the thermocouple was at the center of the tube. The controllers were set at their lowest settings, and power was applied to the tube. The center

zone temperature was then slowly increased until the thermocouple indicated approximately ten degrees below the desired temperature. The thermocouple was then pushed all the was in, and the source zone temperature was slowly increased until the thermocouple indicated about ten degrees less than previously recorded for the center zone. The thermocouple was then withdrawn eleven inches, and the load zone temperature was slowly increased until the thermocouple indicated about the same temperatures as was noted for the source zone. The thermocouple was then pushed to the center, and the temperature adjusted to the desired temperature. Each of the three zones were adjusted by increasing or decreasing the temperature of each zone until the desired temperature was obtained at all three positions. By making very small changes in the three sets of three conrollers, the desired temperature across the eleven inch flat zone in all three tubes, was brought to within plus or minus 0.2 degrees C.

The furnace was then ready for growing oxides, and performing diffusions.

APPENDIX F

PROCESSING SCHEDULE

This appendix summarizes the final fabrication processing steps arrived at through the research of this thesis.

1. Silicon Wafers: Microwave Associates Inc., (MA/COM).

   a. Substrate: p-type, (100), 20 mils, 40 ohm-cm.

   b. Epitaxial Layer: n-type, 2 microns, 0.9 ohm-cm.

2. Source Wafers: PDS, Graphite Products Division, Carborundum Co.

   a. Boron Nitride, grade BN-1100, 3"x.050".

   b. Phosphorous, grade PH-1000, 3"x.060".

3. Furnace Preparation: Thermco Products Co., three inch.

   a. Oxidation Tube: 1050 degrees C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.

   b. P-type Tube: 1050 degrees C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.

   c. N-type Tube: 1000 degrees C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.

4. Initial Oxide: 5000 angstroms.

   a. Initial Wafer Cleaning: Cleaning/etching solution CL1.

b. Oxidation tube.

c. Cycle Times: 20 minutes dry O_2, 48.6 minutes wet O_2, 20 minutes dry O_2.

d. Push/pull: First two feet in/last two feet out at one foot per minute.

e. Bevel and Stain: Check epi diffusion.

f. Measure Oxide with Ellipsometer: First and last wafers in boat.

5. Isolation Diffusion: Boron Source.

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Isolation mask photolithography process.

c. Etch Isolation Pattern: Cleaning/etching solution CL4.

d. P-type Tube: Predeposition.

e. Cycle Time: 40 minutes dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Remove Borosilicate Glass: Cleaning/etching solution CL2.

h. Remove Oxide in Pattern: Cleaning/etching solution CL3.

i. Four-point Probe: Check predep resistivity.

j. Bevel and Stain: Check epi and isolation diffusion depths.

k. Surface Cleaning: Cleaning/etching solution CL3.

l. P-type Tube: Drive

m. Cycle Time: 6 hours, 40 minutes dry N_2.

n. Push/pull: First two feet in/last two feet out at one foot per minute.

o. Four-point Probe: Check drive resistivity.

p. Bevel and Stain: Check epi and isolation diffusion depths.

6. Gate Diffusion: Boron Source.

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Gate mask photolithography process.

c. Etch Gate Pattern: Cleaning/etching solution CL4.

d. P-type Tube: Predeposition.

e. Cycle Time: 15 minutes dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Remove Borosilicate Glass: Cleaning/etching solution CL2.

h. Remove Oxide in Pattern: Cleaning/etching solution CL3.

i. Four-point Probe: Check predep resistivity.

j. Bevel and Stain: Check epi and gate diffusion depths.

k. Surface Cleaning: Cleaning/etching solution CL3.

l. P-type Tube: Drive and gate oxide.

m. Cycle Time: 1 hour dry N_2, 4 minutes dry O_2, 23 minutes wet O_2, 3 minutes dry O_2.

n. Push/pull: First two feet in/last two feet out at one foot per minute.

o. Four-point Probe: Check drive resistivity.

p. Bevel and Stain: Check epi and gate diffusion depths.

q. Ellipsometer: Check field oxide.

7. Source/drain Diffusion: Phosphorous Source.

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Source/drain mask photolithography process.

c. Etch Source/drain Pattern: Cleaning/etching solution CL4.

d. N-type Tube: Predeposition.

e. Cycle Time: 15 minutes dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Four-point Probe: Check predep resistivity.

h. Bevel and Stain: Check epi, gate, and source/drain diffusion depths.

i. Cleaning/etching solution CL3.

j. N-type Tube: Drive and source/drain oxide.

k. Cycle Time: 4 minutes dry O_2, 12 minutes wet O_2, 4 minutes dry O_2.

l. Push/pull: First two feet in/last two feet out at one foot per minute.

m. Bevel and Stain: Check final epi, isolation, gate, and source/drain diffusion depths.

8. Contact Window Openings:

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Contact window mask photolithography process.

c. Etch Contact Window Pattern: Cleaning/etching

solution CL4.

9. Metallization: Consolidated Vacuum Corp. vacuum chamber.

a. 500 angstroms aluminum.

b. 500 angstroms silver.

c. Metal lift off.

APPENDIX G

MULTIPLEXER DESIGN DETAILS

This appendix describes the design and operation of the seven major components of the two NMOS multiplexers: The array electrode, the count selectable counter, the four-bit counter, the row multiplexer, the column multiplexer, the decoder, and the expanded decoder.

Array Electrode

The array electrode (Figure G-1) detects signals of the visual cortex through the large metal pad. At the output of the pad is a pass transistor, acting as a switch. When the switch is off, the output path is open circuited and no output occurs. When the switch is turned on, any signal detected by the pad propagates through the pass transistor and on out the column output to an external recording device.

All the electrode pass transistors in a common row are connected in series by the row select line, which is in turn connected to one of the row multiplexer outputs. While the multiplexer output is low, the row of pass transistors is off. When the multiplexer output goes high, the row of pass transistors is turned on.

In the case of Multiplexer Design I (Figure V-1), the detected signals propagate in parallel, straight to the output pads, and on to an external recording device. In the

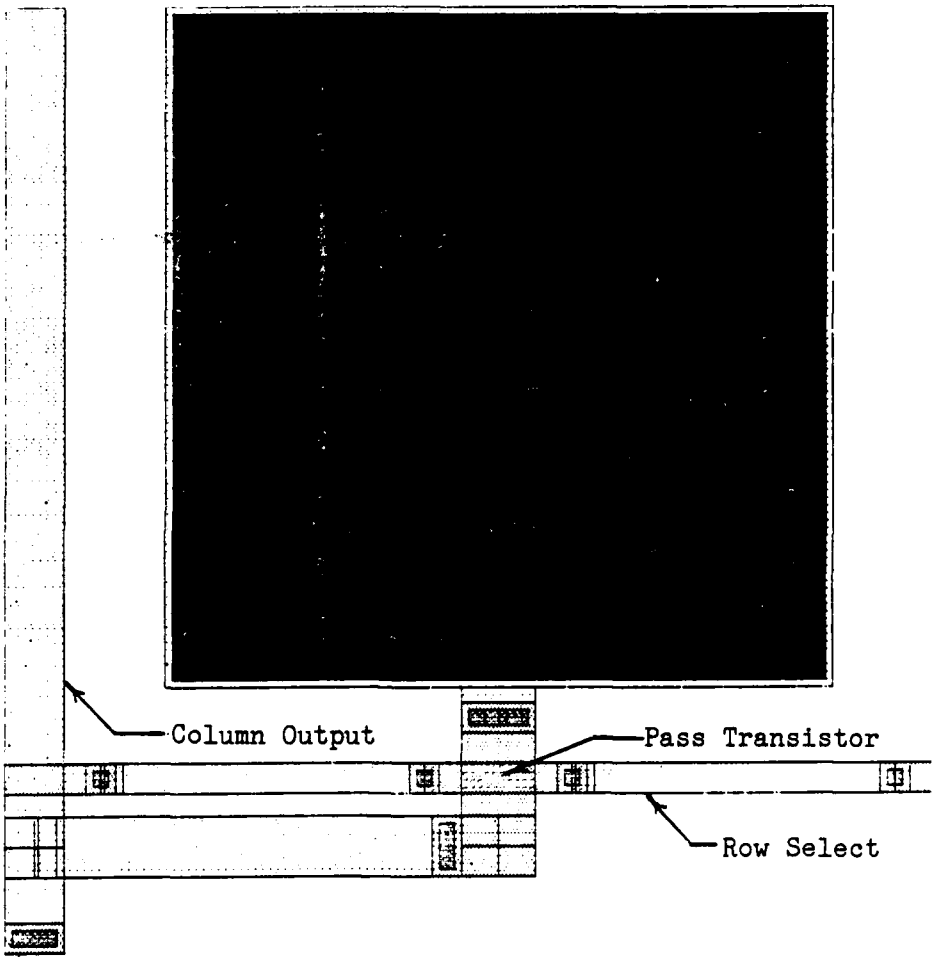

Figure G-1. Array Electrode (Scale: 50 micron per inch).

case of Multiplexer Design II (Figure V-2), the detected signals propagate in parallel until stopped by pass transistors in the column output lines. As each of these column output pass transistors is sequentially turned on by the column multiplexer, the signal appearing on that column propagates to the column output pad, and on to the external recording device.

Converting from the parallel output to a serial output requires only one output signal wire, allowing future expansion of the array without the problem of handling an increasing number of wires.

Count Selectable Counter

The count selectable counter (Figure G-2), a program logic array (PLA) implemented as a finite state machine, operates the same in both multiplexer designs I and II. Four external signals - sync in (SYI), and count select (CS) 0, 1, and 2, and four counter output feedback signals - next state (NS) 0, 1, 2, and 3, are input to the counter by clocking the signals in on ϕ_1 and clocking the signals out on ϕ_2. These clocking signals, generated by NCLK in Multiplexer Design I and NCLK and Mod NCLK in Multiplexer Design II, are non-inverted, and non-overlapping. This allows clocking the counter without creating a race condition, due to the feedback signals.

While SYI is low, the counter, based on the CS inputs, counts sequentially through one of seven predefined

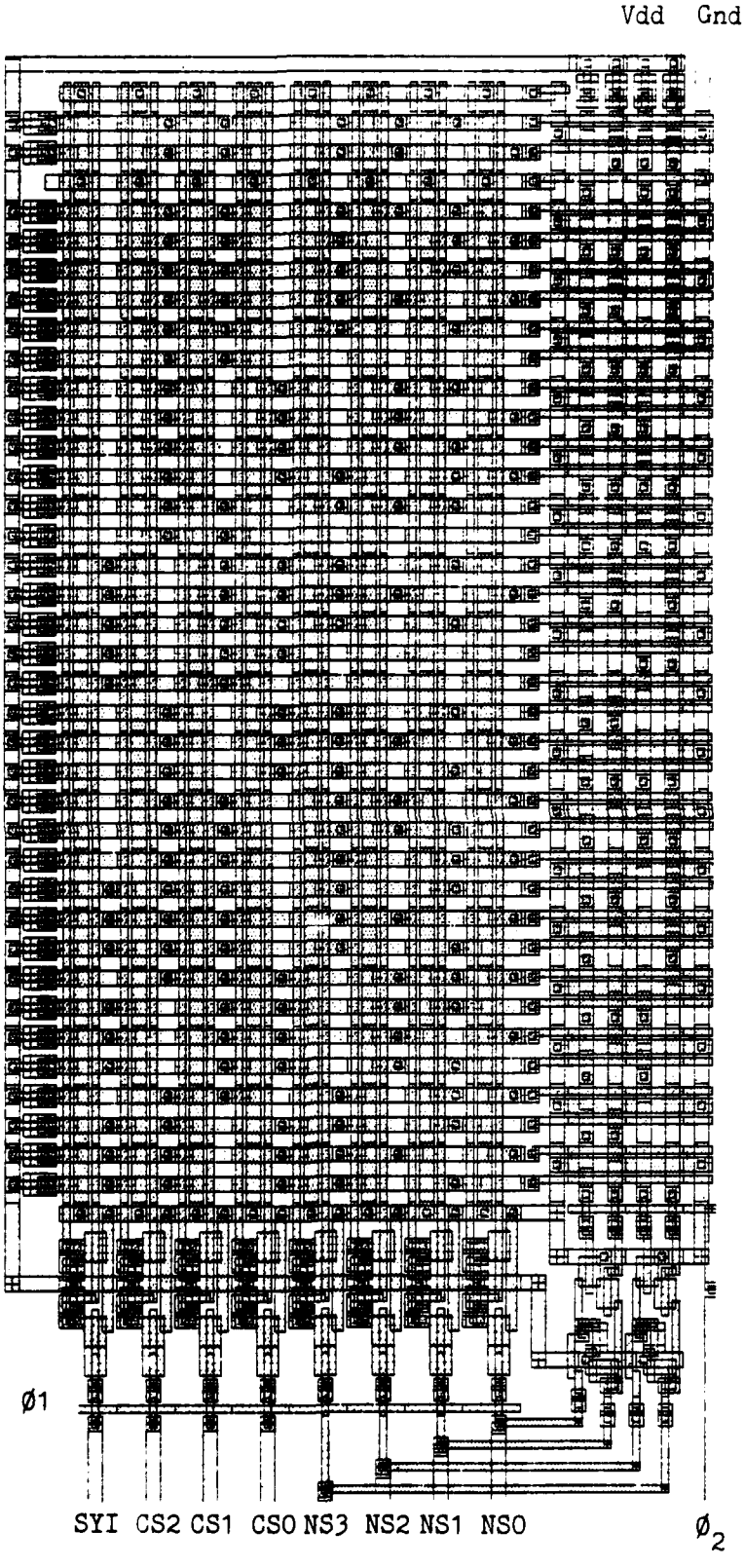

Figure G-2. Count-selectable Counter (Scale: 100 micron per inch).

sequences (Table G-1). The eighth possible CS input combination causes the next state to be "0". While SYI is high, the counter is preset to the lowest count state of the count sequence defined by the CS inputs (Table G-2). This presetting allows the user to begin operation in a known count state.

TABLE G-1

Counter Input/Output (Counting)

Count Select Inputs				Count Output
SYI	CS2	CS1	CS0	
0	0	0	0	0-15
0	0	0	1	0-3
0	0	1	0	4-7
0	0	1	1	8-11
0	1	0	0	12-15
0	1	0	1	0-7
0	1	1	0	8-15
0	1	1	1	0

The selectability of different count sequences permits the use of various combinations of arrays with multiplexer I: One to four - four by four electrode arrays, one or two eight by eight arrays, etc. In addition, the selectability permits monitoring only desired portions of a sixteen by m array with either multiplexer I or II.

The NS outputs, while defining the next count state of

the counter, also input to the row multiplexer and decoder.

TABLE G-2

Counter Input/Output (Presetting)

Count Select Inputs				Count Outputs
SYI	CS2	CS1	CS0	
1	0	0	0	0
1	0	0	1	0
1	0	1	0	4
1	0	1	1	8
1	1	0	0	12
1	1	0	1	0
1	1	1	0	8
1	1	1	1	0

Four-bit Counter

The four-bit counter (Figure G-3), unlike the count selectable counter, is designed to always count 0-15. Also, the four-bit counter's inputs are clocked on $\emptyset_2$, and its outputs are clocked on $\emptyset_1$. These clock phases are not the same signals used to clock the count selectable counter.

The four-bit counter's clocking phases come directly from the clock pad, NCLK (Figure V-2). The most significant output bit (Bit 3) of the four-bit counter goes through an inverter to the modified NCLK pad, which in turn generates a second $\emptyset_1$ and $\emptyset_2$. This design results in the Mod NCLK phases $\emptyset_1$ and $\emptyset_2$ being in correct phase with NCLK $\emptyset_1$ and $\emptyset_2$,

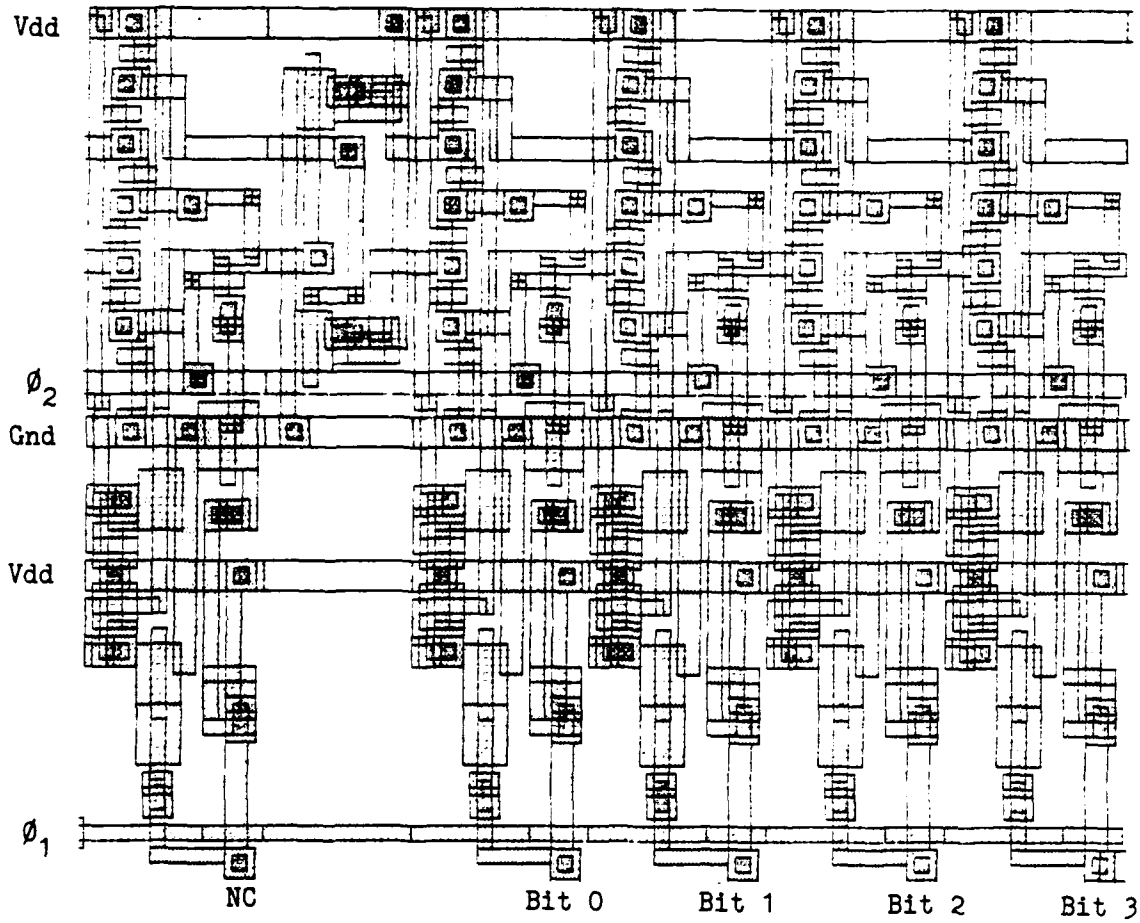

Figure G-3. Four-bit Counter (Scale: 50 micron per inch).

respectively, yet the Mod NCLK phases are clocking sixteen times slower. Ultimately, this difference in clocking rates allows the column multiplexer to select all sixteen outputs during the time any given output of the row multiplexer is high. The four output bits (Bit 0, 1, 2, and 3) of the four-bit counter are connected to the inputs of the column multiplexer.

Row Multiplexer

The row multiplexer (Figure G-4), a PLA, operates the same in both Multiplexer Designs I and II. The NS signals from the counter are input to the multiplexer, and depending on the count state, cause one of the sixteen select out (SO) output lines to go high. The SO lines are connected to a corresponding row select of the array.

The outputs selected by the multiplexer according to the NS inputs, relates directly to Table G-1 and G-2. The outputs are selected sequentially according to the count states of a defined count sequence, or the corresponding output is selected as defined by one of the preset conditions.

In the row multiplexer, the inputs are not clocked, but allowed to propagate through the PLA as fast as possible. This creates no problem as there are no feedback loops in the row multiplexer. The outputs, however, are clocked by $\emptyset_2$ to insure that an output changes only when it is supposed to. This $\emptyset_2$ is the same $\emptyset_2$ used to clock the count

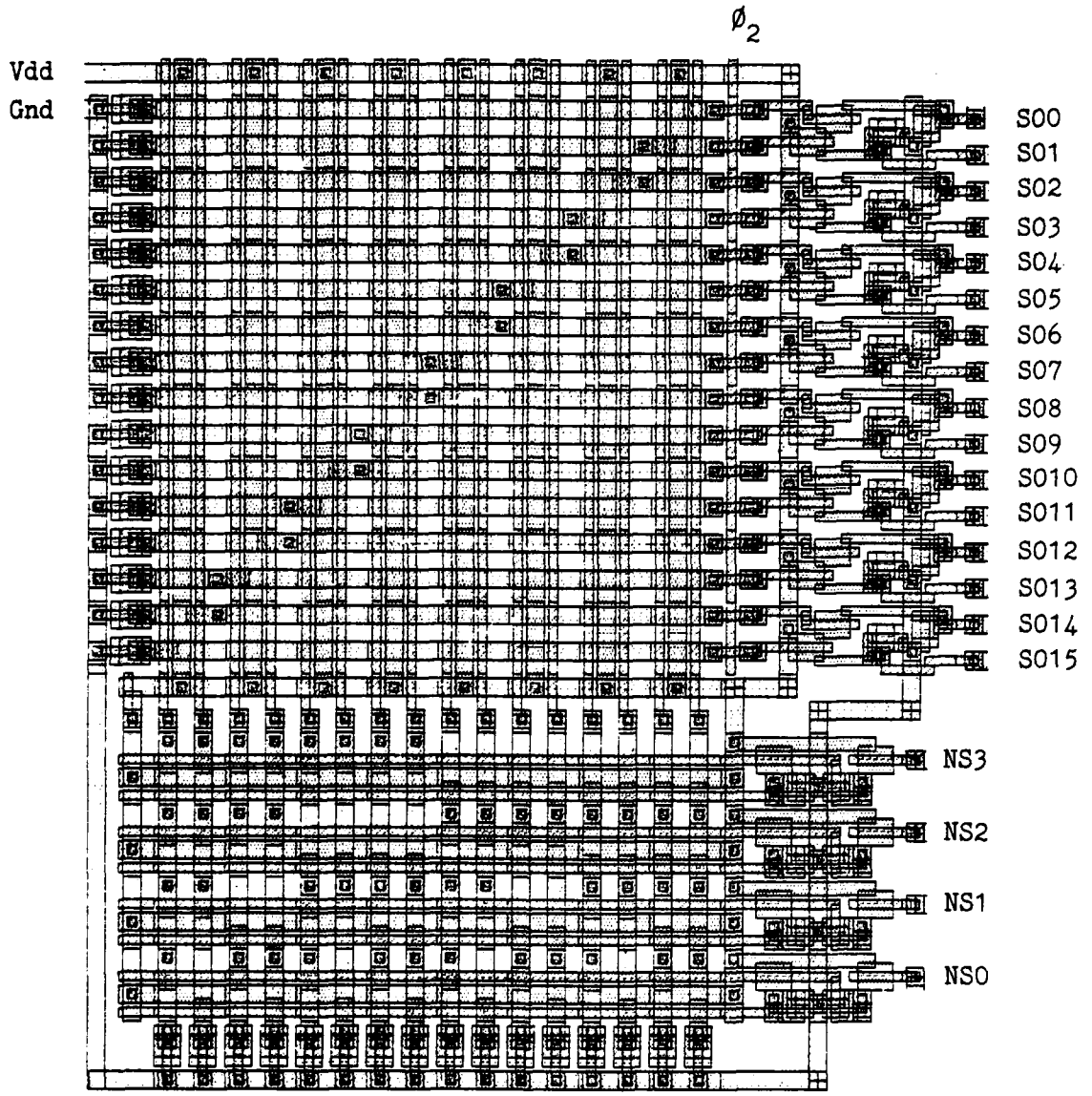

Figure G-4. Row Multiplexer (Scale: 80 micron per inch).

selectable counter outputs.

Column Multiplexer

The column multiplexer (Figure G-5) is identical in design and operation as the row multiplexer. The column multiplexer inputs are the output bits of the four-bit counter, and depending on the count state of the inputs, the column multiplexer selects the corresponding output to go high. Like the row multiplexer, only the column multiplexer's outputs are clocked by ϕ_2. In this instance, however, it is the ϕ_2 generated by NCLK.

The column out (CO) 15 line of the column multiplexer is input to the expanded decoder, indicating to the decoder the completion of an entire count sequence.

Decoder and Expanded Decoder

The decoder and expanded decoder (Figures G-6 and G-7), also PLAs both function the same in Multiplexer Designs I and II respectively. Both decoders input the NS outputs of the count selectable counter, and also input the externally supplied CS signals. In addition, the expanded decoder has an additional input; column output (CO) 15 from the column multiplexer.

When the count state defined by the NS inputs reaches the maximum value of the count sequence determined by the CS inputs, the decoder raises sync out (SYO) as shown in Table G-3. For all other NS inputs, SYO is low. SYO serves two

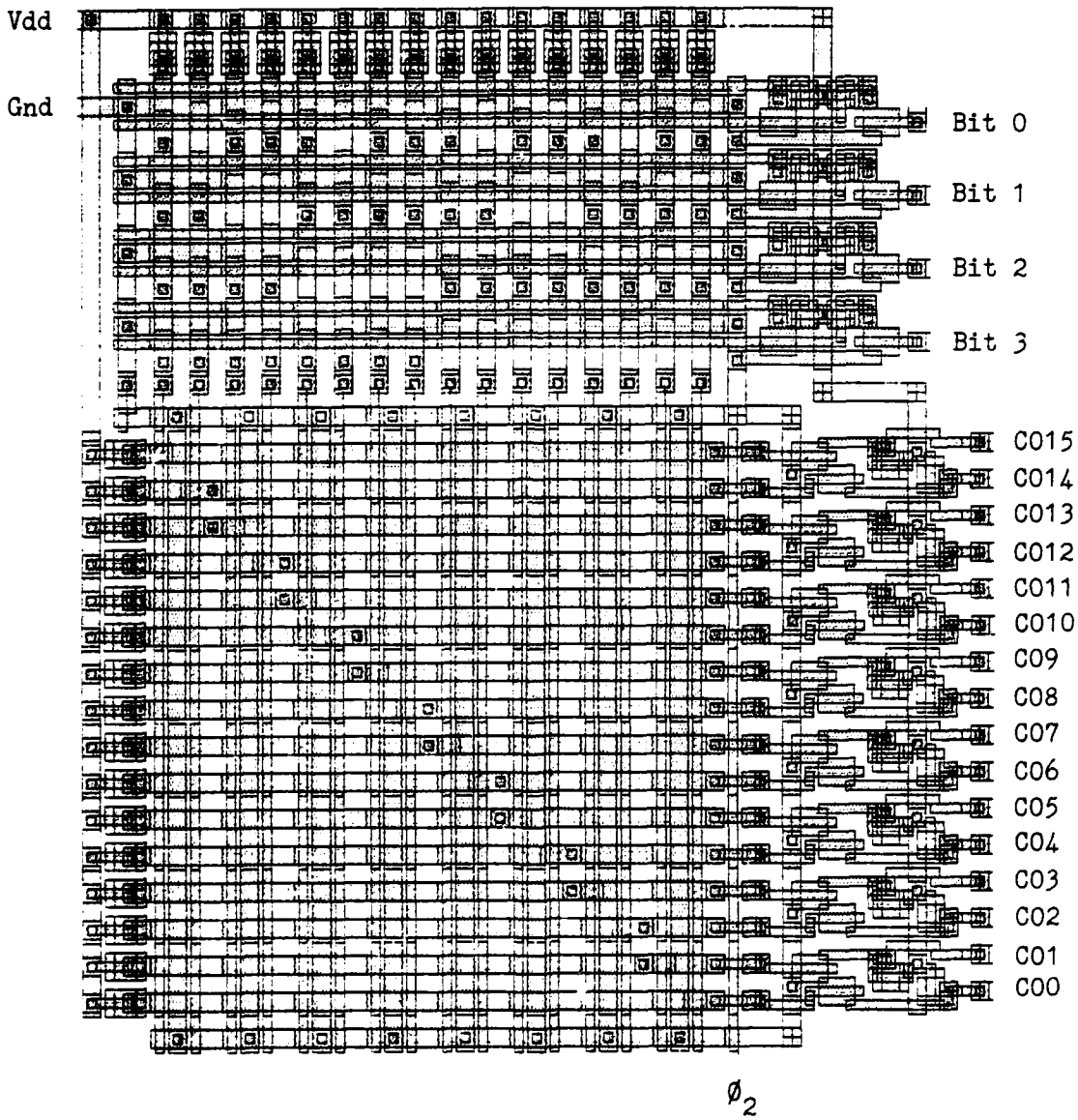

Figure G-5. Column Multiplexer (Scale: 80 micron per inch).

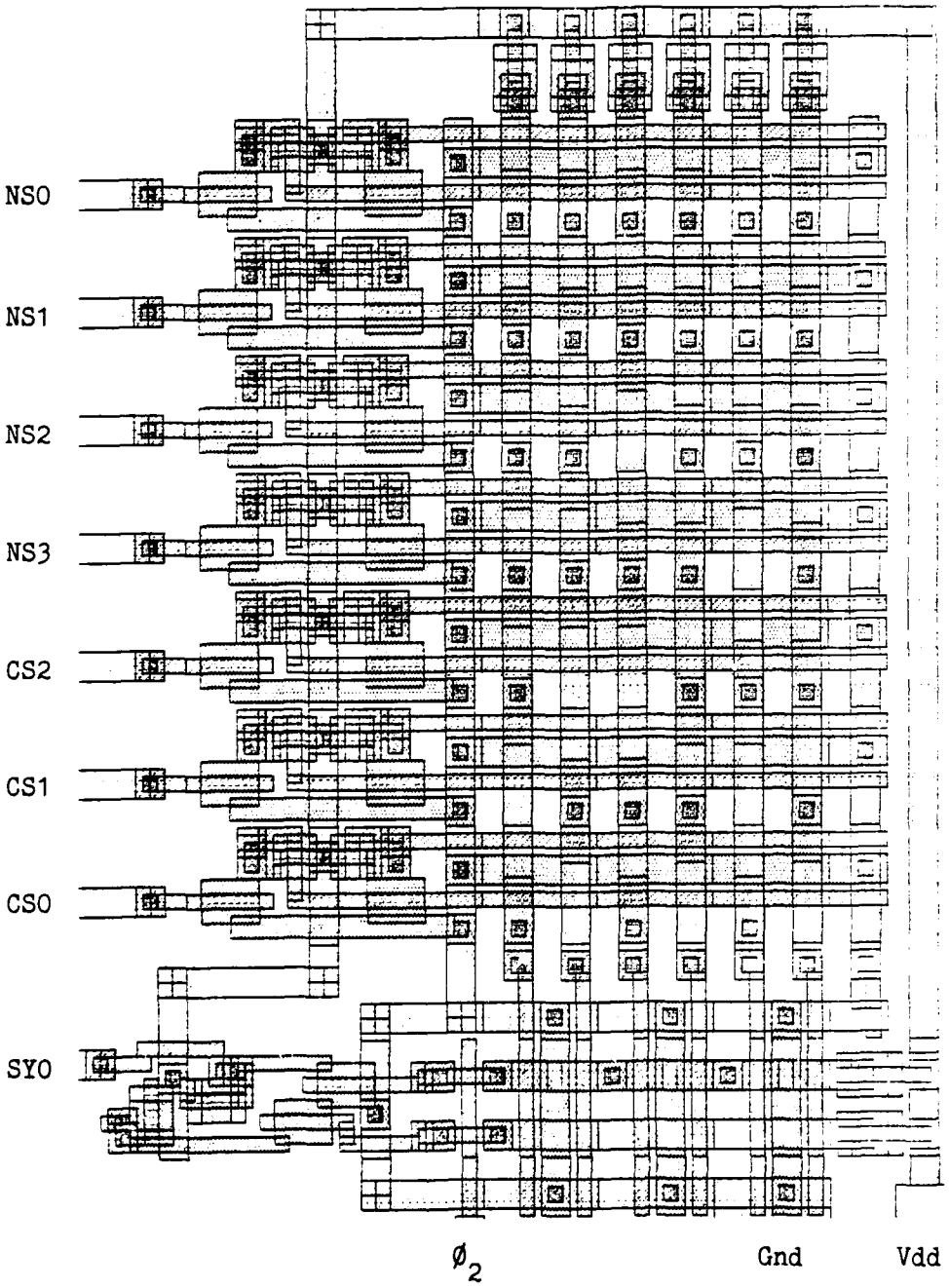

Figure G-6. Decoder (Scale: 50 micron per inch).

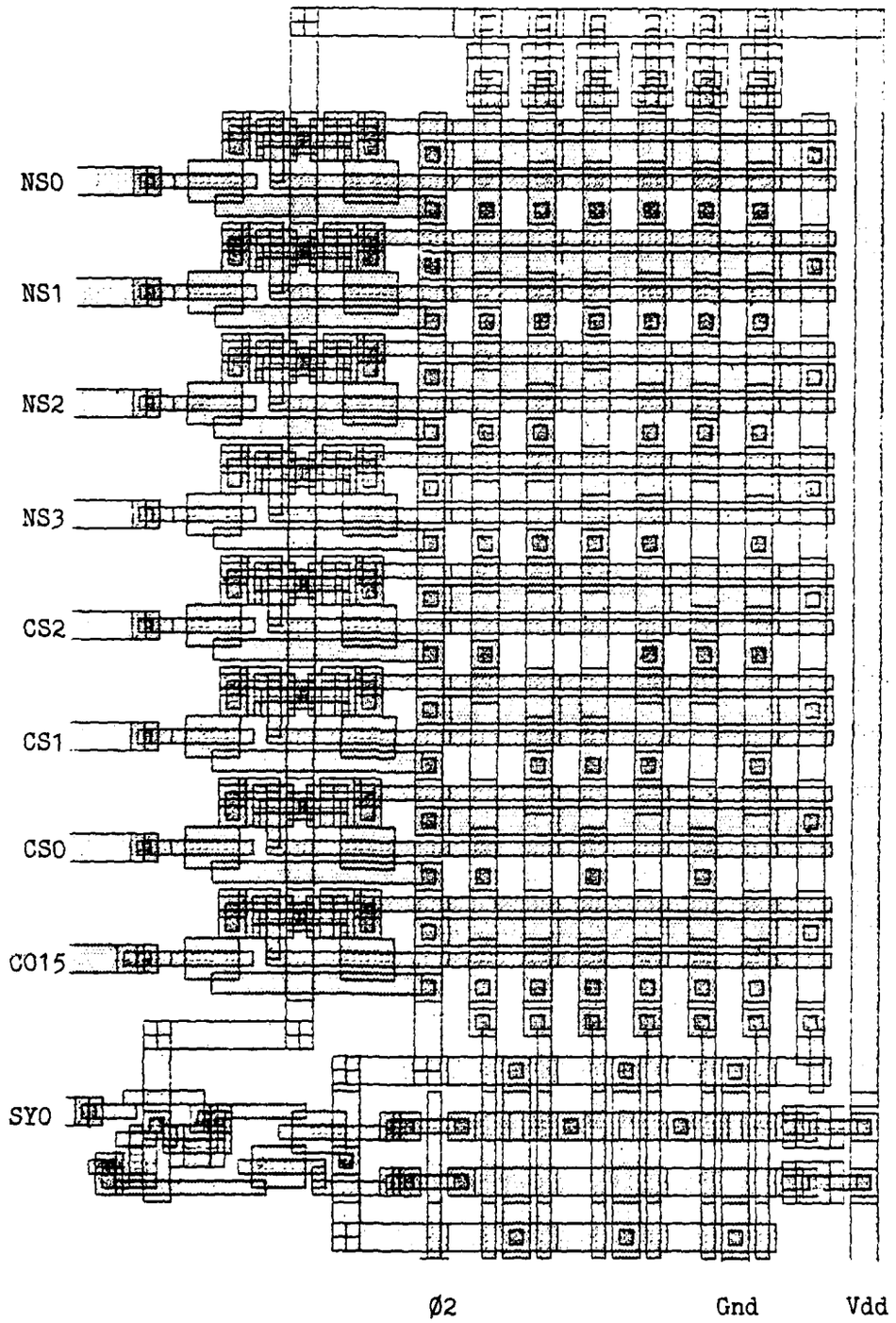

Figure G-7. Expanded Decoder (Scale: 50 micron per inch).

purposes: First, when high, it serves as a timing pulse for an external recording device, and second, it can serve as the SYI signal to other cascaded multiplexer chips, forcing any cascaded counters into synchronization when high.

TABLE G-3

Decoder Input/Output

Inputs							Output
cs2	cs1	cs0	ns3	ns2	ns1	ns0	syo
0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	1
0	1	0	0	1	1	1	1
0	1	1	1	0	1	1	1
1	0	0	1	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	1	1	1	1	1
1	1	1	X	X	X	X	0

The expanded decoder performs the same function, except the SYO goes high only when C015 from the column multiplexer is high as shown in Table G-4.

As with the decoder, the SYO signal of the expanded decoder is low for all other input combinations. As with the multiplexers, neither decoder has clocked inputs. The clocking of the outputs, however, differs somewhat. The decoder used the same ϕ_2 to clock the output as is used to clock the outputs of the count selectable counter. On the

other hand, the expanded decoder uses the same $\emptyset_2$ to clock the ouput as is used to clock the inputs of the count selectable counter. Due to the different overall multiplexer designs, this clocking scheme is necessary to insure proper timing.

TABLE G-4

Expanded Decoder Input/Output

Inputs								Output
cs2	cs1	cs0	ns3	ns2	ns1	ns0	co15	syc
0	0	0	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1
0	1	0	0	1	1	1	1	1
0	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1
1	1	0	1	1	1	1	1	1
1	1	1	X	X	X	X	X	0

Vita

Robert Burton Ballantine was born 4 October 1944 in Miami, Florida. He graduated from Oak Ridge High School, Oak Ridge, Tennessee in June 1962, and enlisted in the Air Force in October 1962. After Basic Military Training at Lackland AFB, Texas, he attended technical training at Sheppard AFB, Texas, to perform duties as a Ballistic Missile Analyst Technician on the Titan II ICBM. Subsequent tours of duty included: 381st Strategic Missile Wing, McConnell AFB, Kansas; 314th Tactical Airlift Wing, Ching Chuan Kang, Republic of China Air Base, Taichung, Taiwan; 8th Tactical Fighter Wing, Ubon Royal Thai Air Base, Ubon, Thailand; and 363rd Civil Engineering Squadron, Shaw AFB, South Carolina. While at Ubon, he attended University of Maryland on base courses, and upon reassignment to Shaw AFB, attended the University of South Carolina, receiving a Bachelor of Science in Electrical Engineering degree in December 1977. He was accepted into Officer Training School in February 1978, and received a commission as a Second Lieutenent in May that year. He was then assigned to the Flight Dynamics Laboratory, Wright-Patterson AFB, Ohio, as a Flight Control Systems Integration Engineer until his assignment to the Air Force Institute of Technology in June 1982.

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Block 19 (cont)

A new JFET multielectrode array, consisting of a four by four array and sixteen junction field effect transistors, has been fabricated. Changes in the fabrication processes include: The use of three inch wafers, in lieu of one and one quarter inch wafers; positive photoresist, instead of negative photoresist; different impurity sources; different diffusion times and temperatures; and a two metal metallization layer, versus a four metal metallization layer.

In addition, two unique NMOS multiplexer circuits have been designed for use with either the JFET multielectrode array, or an NMOS multielectrode array. The first multiplexer circuit contains a count-selectable counter, a one of sixteen output multiplexer, a decoder for generating a sync signal, and a sixteen by sixteen multielectrode array, all on a single chip. In addition, the array can be separated from the chip, permitting the use of the remaining circuitry with other types and sizes of arrays.

The second multiplexer circuit contains the same features of the first multiplexer, plus an additional one of sixteen output multiplexer and a four-bit counter. With this chip, however, the array can not be separated from the remaining circuitry.